

CONTENT	SHEET
Cover Sheet, Block Diagram	1-2
Intel LGA1366 CPU	3-8
DDR3 Chanel-A / Chanel-B / Chanel-C	9-11
Intel IOH 36S	12-19
ICH9R / ICH10R	20-22
Clock Gen ICS9LPRS113	23
PCI SLOT1 , 2	24
PCI-E X16 SLOT1 , 2	25
PCI-E X4 / X1 SLOT	26
SIO-Fintek F71882F	27
LAN1 / LAN2 - RTL8111C	28-29
Audio Codec ALC888/888T	30
1394 Controller - JMB381	31
JMB-363 E-SATA X2/ IDE X1	32
Sil5723 - RAID SATA x2	33
USB Connector	34
VRD11.1 - ISL6336 5-Phase	35
Phase Dropping & DOT	36
CPU_VTT - ISL6314 1-Phase	37
ACPI Controller UPI	38
NB Core Power & DDR Power	39
ATX Connector/F_Panel	40
ICH SATA / FAN Control	41
GPIO Controller / EMI	42
XDP PORT/ Manual Parts	43-44
GPIO Setting / PCI Routing / Power Map	45-46
Reset & PWROK Map / 6-layer PCB Stack-up	47-48
Revision History	49

MS-7520

ATX Version: 0A

CPU: Nehalem-EP 1S, BloomField Processors In LGA1366 Package.

System Chipset:

Intel Tlyersburg I/O Hub 36S (North Bridge)

Intel ICH9R/ICH10R (South Bridge)

On Board Device:

CLOCK Gen -- ICS 9LPRS113

LPC Super I/O -- Fintek F71882F

Dual LAN --Realtek 8111C X2

HD Audio Codec -- RTL888/888T

1394 Controller -- JMB381

PCIE to 1PATA/2SATA Bridge -- JMB363

SATA RAID-- Sil5723

Main Memory:

3-Channel A / B / C DDR-III * 6

Expansion Slots:

PCI EXPRESS X16 SLOT *2

PCI EXPRESS X4 SLOT*1

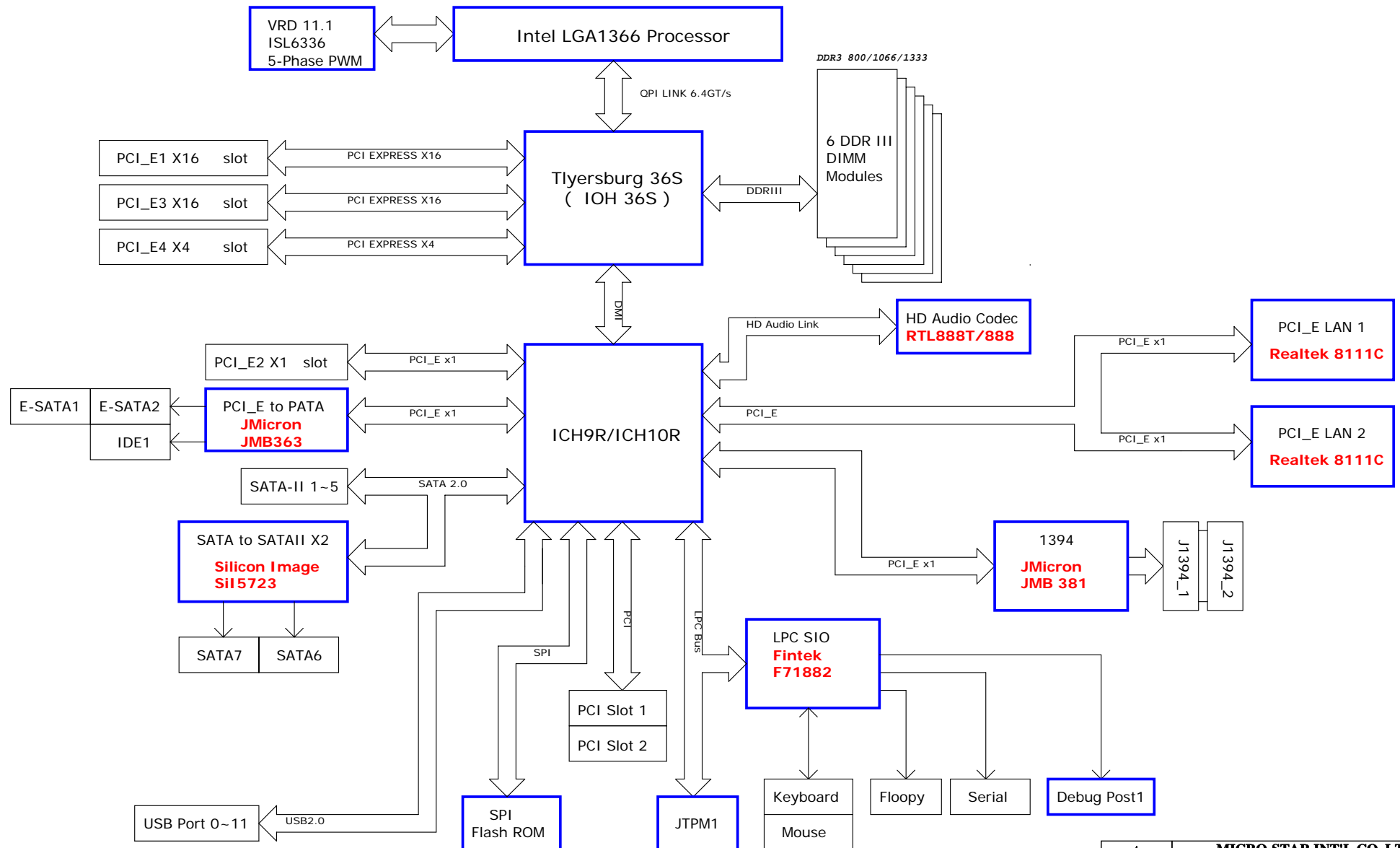
PCI EXPRESS X1 SLOT * 1

PCI SLOT * 2

PWM: VR11.1 Intersil ISL6336 (5 Phases)

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Size Custom	Document Description COVER SHEET		Rev 0A
Date: Thursday, March 13, 2008	Sheet	1	of 49

Block Diagram



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MS-7520

Size	Document Description	Rev
Custom	BLOCK DIAGRAM	0A
Date: Thursday, March 13, 2008	Sheet 2 of 49	

(9) DATA_A[0..63] <<>

U71A 1 OF 12			
DATA A0 W41	DDR0_DQ_0	DDR0_DQS_P0	T43 DQS A0 <>> DQS A0 (9)
DATA A1 V41	DDR0_DQ_1	DDR0_DQS_N0	U43 DQS A#0 <>> DQS A#0 (9)
DATA A2 R42	DDR0_DQ_2		
DATA A3 R42	DDR0_DQ_3	DDR0_DQS_P1	L41 DQS A1 <>> DQS A1 (9)
DATA A4 W40	DDR0_DQ_4	DDR0_DQS_N1	M41 DQS A#1 <>> DQS A#1 (9)
DATA A5 W42	DDR0_DQ_5		
DATA A6 U41	DDR0_DQ_6		
DATA A7 T42	DDR0_DQ_7	DDR0_DQS_P2	F41 DQS A2 <>> DQS A2 (9)
DATA A8 N41	DDR0_DQ_8	DDR0_DQS_N2	G41 DQS A#2 <>> DQS A#2 (9)
DATA A9 N43	DDR0_DQ_9		
DATA A10 K42	DDR0_DQ_10	DDR0_DQS_P3	B39 DQS A3 <>> DQS A3 (9)
DATA A11 K43	DDR0_DQ_11	DDR0_DQS_N3	B40 DQS A#3 <>> DQS A#3 (9)
DATA A12 P42	DDR0_DQ_12		
DATA A13 P41	DDR0_DQ_13	DDR0_DQS_P4	E3 DQS A4 <>> DQS A4 (9)
DATA A14 L42	DDR0_DQ_14	DDR0_DQS_N4	E4 DQS A#4 <>> DQS A#4 (9)
DATA A15 L43	DDR0_DQ_15		
DATA A16 H41	DDR0_DQ_16	DDR0_DQS_P5	K2 DQS A5 <>> DQS A5 (9)
DATA A17 H43	DDR0_DQ_17	DDR0_DQS_N5	K3 DQS A#5 <>> DQS A#5 (9)
DATA A18 E42	DDR0_DQ_18		
DATA A19 E43	DDR0_DQ_19	DDR0_DQS_P6	R2 DQS A6 <>> DQS A6 (9)
DATA A20 J42	DDR0_DQ_20	DDR0_DQS_N6	R3 DQS A#6 <>> DQS A#6 (9)
DATA A21 J41	DDR0_DQ_21		
DATA A22 F43	DDR0_DQ_22	DDR0_DQS_P7	W2 DQS A7 <>> DQS A7 (9)
DATA A23 F42	DDR0_DQ_23	DDR0_DQS_N7	W1 DQS A#7 <>> DQS A#7 (9)
DATA A24 D40	DDR0_DQ_24		
DATA A25 C41	DDR0_DQ_25	DDR0_DQS_P8	D34 <>>
DATA A26 A38	DDR0_DQ_26	DDR0_DQS_N8	D35 <>>
DATA A27 D37	DDR0_DQ_27		
DATA A28 D37	DDR0_DQ_28	DDR0_DQS_P9	V43 <>>
DATA A29 D42	DDR0_DQ_29	DDR0_DQS_N9	V42 <>>
DATA A30 C38	DDR0_DQ_30		
DATA A31 B38	DDR0_DQ_31	DDR0_DQS_P10	N42 <>>
DATA A32 B5	DDR0_DQ_32	DDR0_DQS_N10	M43 <>>
DATA A33 C4	DDR0_DQ_33		
DATA A34 F1	DDR0_DQ_34	DDR0_DQS_P11	H42 <>>
DATA A35 G3	DDR0_DQ_35	DDR0_DQS_N11	G43 <>>
DATA A36 B6	DDR0_DQ_36		
DATA A37 C6	DDR0_DQ_37	DDR0_DQS_P12	D39 <>>
DATA A38 F3	DDR0_DQ_38	DDR0_DQS_N12	C39 <>>
DATA A39 F2	DDR0_DQ_39		
DATA A40 H2	DDR0_DQ_40	DDR0_DQS_P13	D5 <>>
DATA A41 H1	DDR0_DQ_41	DDR0_DQS_N13	D4 <>>
DATA A42 L1	DDR0_DQ_42		
DATA A43 M1	DDR0_DQ_43	DDR0_DQS_P14	J2 <>>
DATA A44 G1	DDR0_DQ_44	DDR0_DQS_N14	J1 <>>
DATA A45 H3	DDR0_DQ_45		
DATA A46 L3	DDR0_DQ_46	DDR0_DQS_P15	P2 <>>
DATA A47 L2	DDR0_DQ_47	DDR0_DQS_N15	P1 <>>
DATA A48 N1	DDR0_DQ_48		
DATA A49 N1	DDR0_DQ_49	DDR0_DQS_P16	V2 <>>
DATA A50 T1	DDR0_DQ_50	DDR0_DQS_N16	V3 <>>
DATA A51 T2	DDR0_DQ_51		
DATA A52 M3	DDR0_DQ_52	DDR0_DQS_P17	B36 <>>
DATA A53 N3	DDR0_DQ_53	DDR0_DQS_N17	B35 <>>
DATA A54 R4	DDR0_DQ_54		
DATA A55 T3	DDR0_DQ_55		
DATA A56 U4	DDR0_DQ_56		
DATA A57 V1	DDR0_DQ_57		
DATA A58 Y2	DDR0_DQ_58		
DATA A59 Y3	DDR0_DQ_59		
DATA A60 U1	DDR0_DQ_60		
DATA A61 U3	DDR0_DQ_61		
DATA A62 V4	DDR0_DQ_62		
DATA A63 W4	DDR0_DQ_63		
LGA_1366			
DDR0_ECC_0 <>> C36			
DDR0_ECC_1 <>> A36			
DDR0_ECC_2 <>> E32			
DDR0_ECC_3 <>> C33			
DDR0_ECC_4 <>> A37			
DDR0_ECC_5 <>> B34			
DDR0_ECC_6 <>> B34			
DDR0_ECC_7 <>> C34			

(10) DATA_B[0..63] <>>

U71B 2 OF 12			
DATA B0 AA37	DDR1_DQ_0		
DATA B1 AA36	DDR1_DQ_1		
DATA B2 Y36	DDR1_DQ_2		
DATA B3 Y34	DDR1_DQ_3		
DATA B4 AA35	DDR1_DQ_4		
DATA B5 AB36	DDR1_DQ_5		
DATA B6 Y38	DDR1_DQ_6		
DATA B7 Y40	DDR1_DQ_7		
DATA B8 P34	DDR1_DQ_8		
DATA B9 P35	DDR1_DQ_9		
DATA B10 P38	DDR1_DQ_10		
DATA B11 N38	DDR1_DQ_11		
DATA B12 R34	DDR1_DQ_12		
DATA B13 R35	DDR1_DQ_13		
DATA B14 N37	DDR1_DQ_14		
DATA B15 N38	DDR1_DQ_15		
DATA B16 M35	DDR1_DQ_16		
DATA B17 M34	DDR1_DQ_17		
DATA B18 K35	DDR1_DQ_18		
DATA B19 J35	DDR1_DQ_19		
DATA B20 N34	DDR1_DQ_20		
DATA B21 M36	DDR1_DQ_21		
DATA B22 J36	DDR1_DQ_22		
DATA B23 K36	DDR1_DQ_23		
DATA B24 H33	DDR1_DQ_24		
DATA B25 L33	DDR1_DQ_25		
DATA B26 K32	DDR1_DQ_26		
DATA B27 J32	DDR1_DQ_27		
DATA B28 H34	DDR1_DQ_28		
DATA B29 H34	DDR1_DQ_29		
DATA B30 L32	DDR1_DQ_30		
DATA B31 K30	DDR1_DQ_31		
DATA B32 E8	DDR1_DQ_32		
DATA B33 E5	DDR1_DQ_33		
DATA B34 E5	DDR1_DQ_34		
DATA B35 F10	DDR1_DQ_35		
DATA B36 F8	DDR1_DQ_36		
DATA B37 D6	DDR1_DQ_37		
DATA B38 F6	DDR1_DQ_38		
DATA B39 H6	DDR1_DQ_39		
DATA B40 J6	DDR1_DQ_40		
DATA B41 G4	DDR1_DQ_41		
DATA B42 G4	DDR1_DQ_42		
DATA B43 H4	DDR1_DQ_43		
DATA B44 G9	DDR1_DQ_44		
DATA B45 H9	DDR1_DQ_45		
DATA B46 G5	DDR1_DQ_46		
DATA B47 J5	DDR1_DQ_47		
DATA B48 K4	DDR1_DQ_48		
DATA B49 K5	DDR1_DQ_49		
DATA B50 R5	DDR1_DQ_50		
DATA B51 T5	DDR1_DQ_51		
DATA B52 J4	DDR1_DQ_52		
DATA B53 R8	DDR1_DQ_53		
DATA B54 R7	DDR1_DQ_54		
DATA B55 W7	DDR1_DQ_55		
DATA B56 W7	DDR1_DQ_56		
DATA B57 Y10	DDR1_DQ_57		
DATA B58 W10	DDR1_DQ_58		
DATA B59 V9	DDR1_DQ_59		
DATA B60 W5	DDR1_DQ_60		
DATA B61 AA7	DDR1_DQ_61		
DATA B62 AA7	DDR1_DQ_62		
DATA B63 W9	DDR1_DQ_63		
LGA_1366			
DDR1_ECC_0 <>> D36			
DDR1_ECC_1 <>> E36			
DDR1_ECC_2 <>> E33			
DDR1_ECC_3 <>> G36			
DDR1_ECC_4 <>> E37			
DDR1_ECC_5 <>> E34			
DDR1_ECC_6 <>> E34			
DDR1_ECC_7 <>> G35			

(11) DATA_C[0..63] <>>

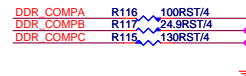
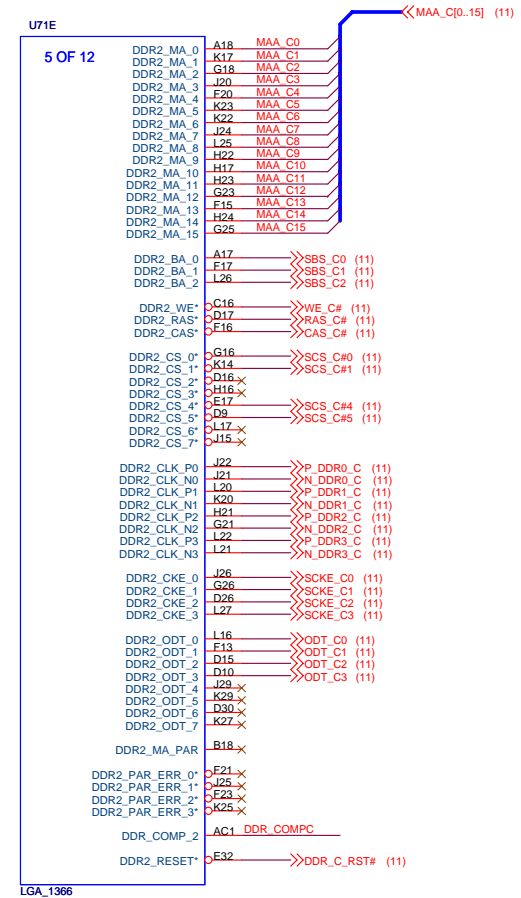
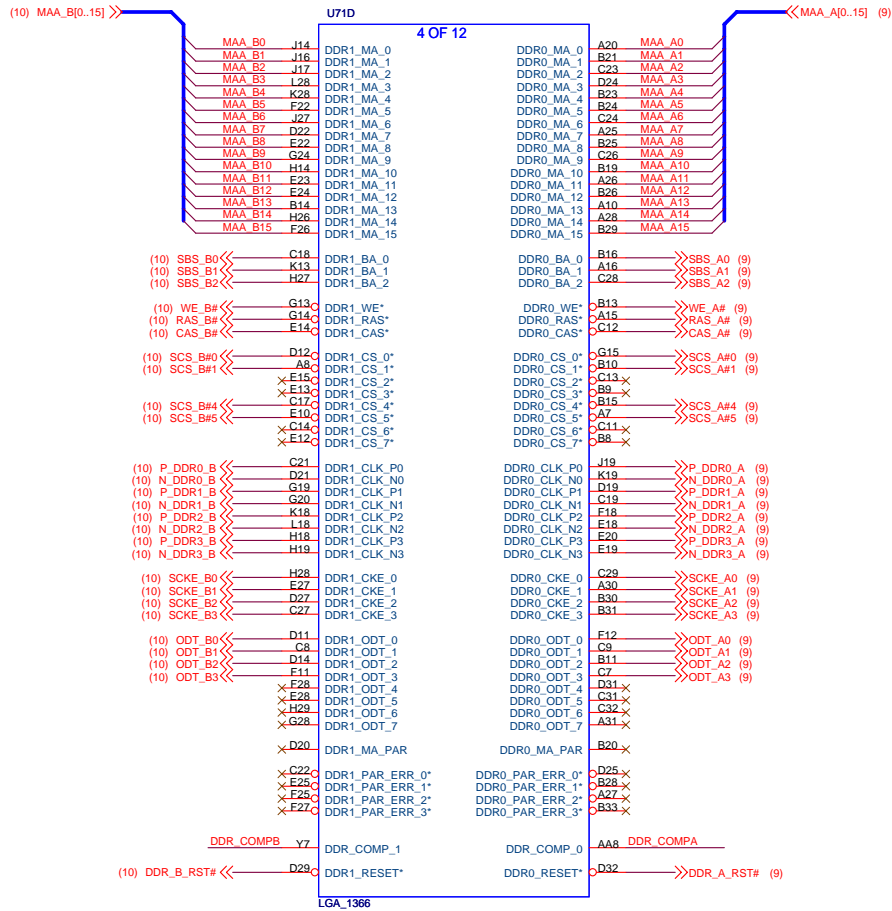
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DATA C0 W34	DDR2_DQ_0	DDR2_DQS_P0	W37 DQS C0 <>> DQS_C0 (11)
DATA C1 W35	DDR2_DQ_1	DDR2_DQS_N0	W36 DQS C#0 <>> DQS_C#0 (11)
DATA C2 V36	DDR2_DQ_2		
DATA C3 U36	DDR2_DQ_3	DDR2_DQS_P1	T37 DQS C1 <>> DQS_C1 (11)
DATA C4 U34	DDR2_DQ_4	DDR2_DQS_N1	T38 DQS C#1 <>> DQS_C#1 (11)
DATA C5 V34	DDR2_DQ_5		
DATA C6 V37	DDR2_DQ_6		
DATA C7 V39	DDR2_DQ_7	DDR2_DQS_P2	K40 DQS C2 <>> DQS_C2 (11)
DATA C8 U38	DDR2_DQ_8	DDR2_DQS_N2	K39 DQS C#2 <>> DQS_C#2 (11)
DATA C9 U39	DDR2_DQ_9		
DATA C10 R39	DDR2_DQ_10	DDR2_DQS_P3	E39 DQS C3 <>> DQS_C3 (11)
DATA C11 T36	DDR2_DQ_11	DDR2_DQS_N3	E40 DQS C#3 <>> DQS_C#3 (11)
DATA C12 W39	DDR2_DQ_12		
DATA C13 V39	DDR2_DQ_13	DDR2_DQS_P4	J10 DQS C4 <>> DQS_C4 (11)
DATA C14 T41	DDR2_DQ_14	DDR2_DQS_N4	J9 DQS C#4 <>> DQS_C#4 (11)
DATA C15 R40	DDR2_DQ_15		
DATA C16 M39	DDR2_DQ_16	DDR2_DQS_P5	L7 DQS C5 <>> DQS_C5 (11)
DATA C17 M40	DDR2_DQ_17	DDR2_DQS_N5	K7 DQS C#5 <>> DQS_C#5 (11)
DATA C18 J40	DDR2_DQ_18		
DATA C19 J39	DDR2_DQ_19	DDR2_DQS_P6	P6 DQS C6 <>> DQS_C6 (11)
DATA C20 P40	DDR2_DQ_20	DDR2_DQS_N6	P5 DQS C#6 <>> DQS_C#6 (11)
DATA C21 N36	DDR2_DQ_21		
DATA C22 L40	DDR2_DQ_22	DDR2_DQS_P7	U8 DQS C7 <>> DQS_C7 (11)
DATA C23 K38	DDR2_DQ_23	DDR2_DQS_N7	T8 DQS C#7 <>> DQS_C#7 (11)
DATA C24 G40	DDR2_DQ_24		
DATA C25 F40	DDR2_DQ_25	DDR2_DQS_P8	G29 <>>
DATA C26 J37	DDR2_DQ_26	DDR2_DQS_N8	G30 <>>
DATA C27 H37	DDR2_DQ_27		
DATA C28 H39	DDR2_DQ_28	DDR2_DQS_P9	U35 <>>
DATA C29 G39	DDR2_DQ_29	DDR2_DQS_N9	T35 <>>
DATA C30 F38	DDR2_DQ_30		
DATA C31 E38	DDR2_DQ_31	DDR2_DQS_P10	U40 <>>
DATA C32 K12	DDR2_DQ_32	DDR2_DQS_N10	T40 <>>
DATA C33 J12	DDR2_DQ_33		
DATA C34 H13	DDR2_DQ_34	DDR2_DQS_P11	M38 <>>
DATA C35 L13	DDR2_DQ_35	DDR2_DQS_N11	L38 <>>
DATA C36 G11	DDR2_DQ_36		
DATA C37 G10	DDR2_DQ_37	DDR2_DQS_P12	H38 <>>
DATA C38 H12	DDR2_DQ_38	DDR2_DQS_N12	G38 <>>
DATA C39 L12	DDR2_DQ_39		
DATA C40 L10	DDR2_DQ_40	DDR2_DQS_P13	H11 <>>
DATA C41 K10	DDR2_DQ_41	DDR2_DQS_N13	J11 <>>
DATA C42 M9	DDR2_DQ_42		
DATA C43 N9	DDR2_DQ_43	DDR2_DQS_P14	K9 <>>
DATA C44 L11	DDR2_DQ_44	DDR2_DQS_N14	K8 <>>
DATA C45 M10	DDR2_DQ_45		
DATA C46 L8	DDR2_DQ_46	DDR2_DQS_P15	N4 <>>
DATA C47 M8	DDR2_DQ_47	DDR2_DQS_N15	P4 <>>
DATA C48 E7	DDR2_DQ_48		
DATA C49 N6	DDR2_DQ_49	DDR2_DQS_P16	V6 <>>
DATA C50 P9	DDR2_DQ_50	DDR2_DQS_N16	V7 <>>
DATA C51 P10	DDR2_DQ_51		
DATA C52 N8	DDR2_DQ_52	DDR2_DQS_P17	H31 <>>
DATA C53 N7	DDR2_DQ_53	DDR2_DQS_N17	G31 <>>
DATA C54 R10	DDR2_DQ_54		
DATA C55 R9	DDR2_DQ_55		
DATA C56 U5	DDR2_DQ_56		
DATA C57 U6	DDR2_DQ_57		
DATA C58 T10	DDR2_DQ_58		
DATA C59 U10	DDR2_DQ_59		
DATA C60 T6	DDR2_DQ_60		
DATA C61 T7	DDR2_DQ_61		
DATA C62 V8	DDR2_DQ_62		
DATA C63 U9	DDR2_DQ_63		
LGA_1366			
DDR2_ECC_0 <>> H32			
DDR2_ECC_1 <>> E33			
DDR2_ECC_2 <>> E29			
DDR2_ECC_3 <>> E30			
DDR2_ECC_4 <>> J31			
DDR2_ECC_5 <>> J30			
DDR2_ECC_6 <>> F31			
DDR2_ECC_7 <>> F30			

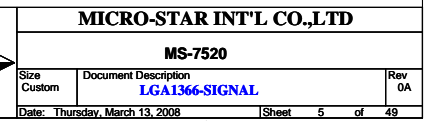
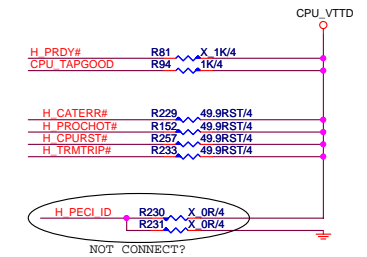


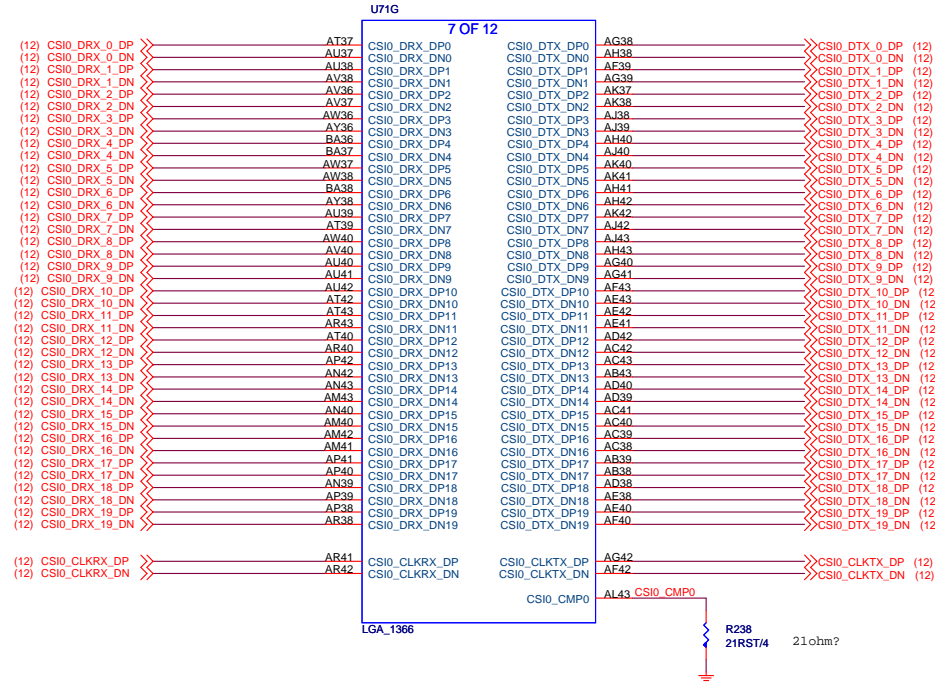
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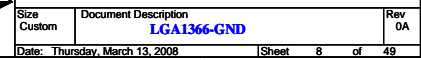
MS-7520

Size Custom	Document Description LGA1366-MEM DQ/DQS	Rev 0A
Date: Thursday, March 13, 2008		Sheet 3 of 49

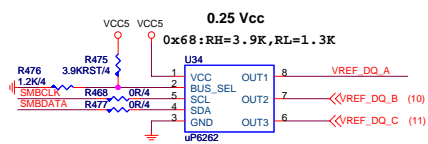
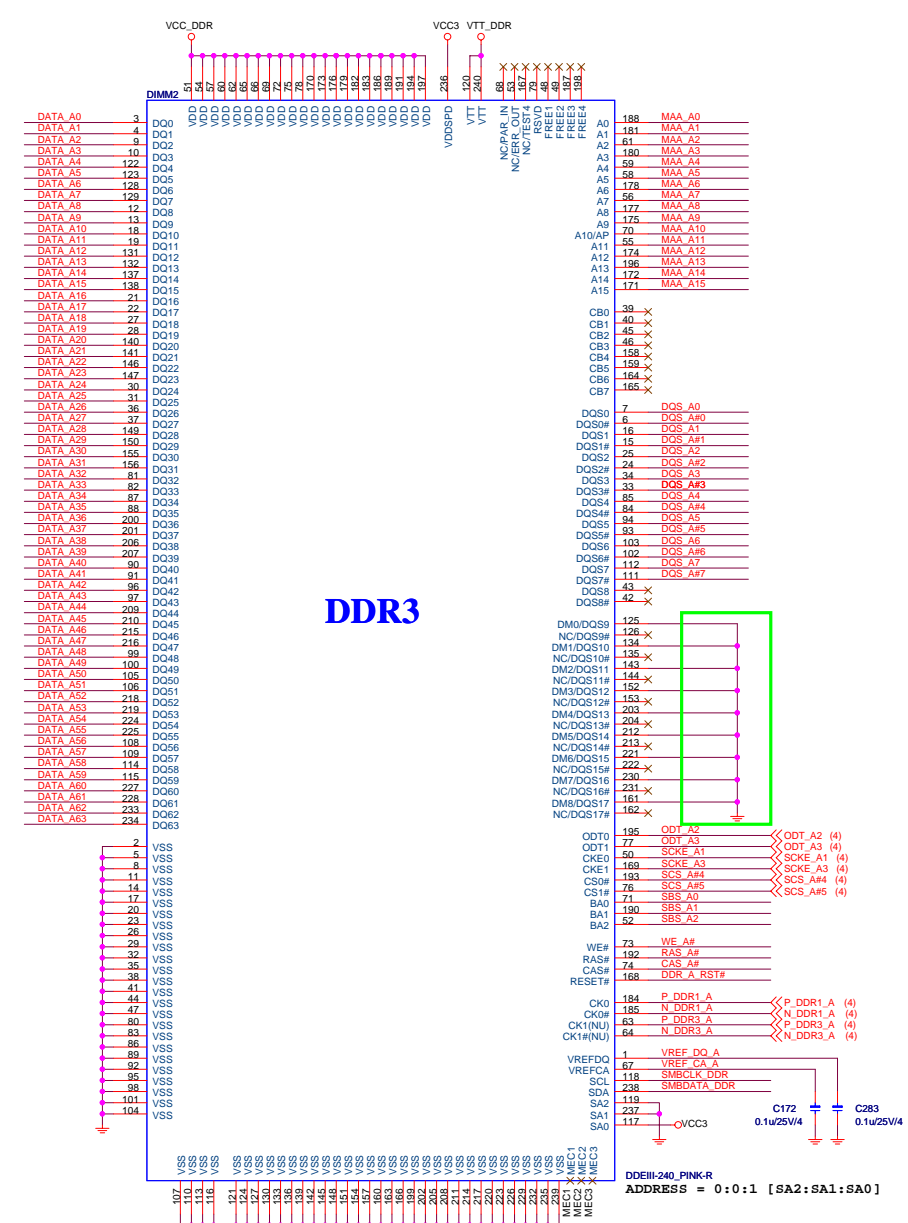









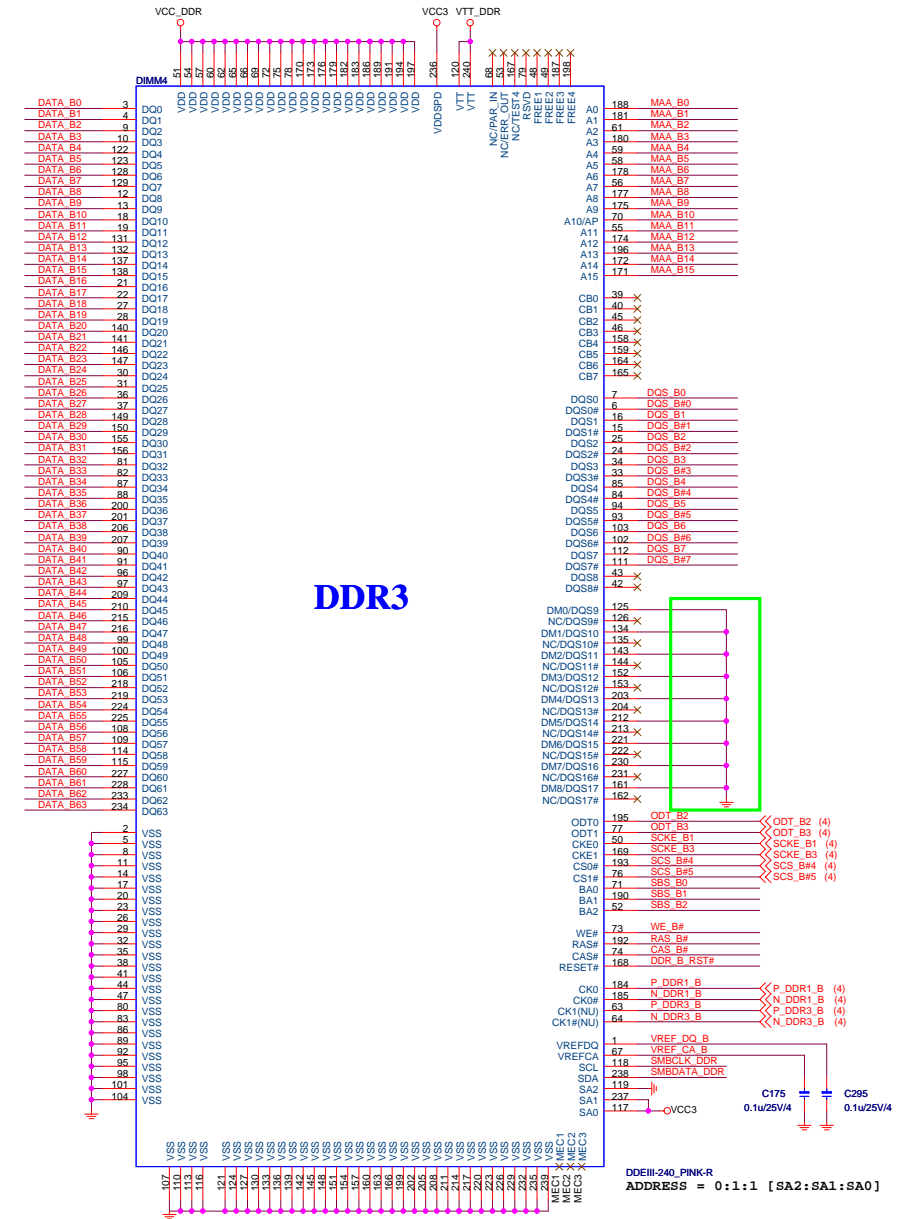
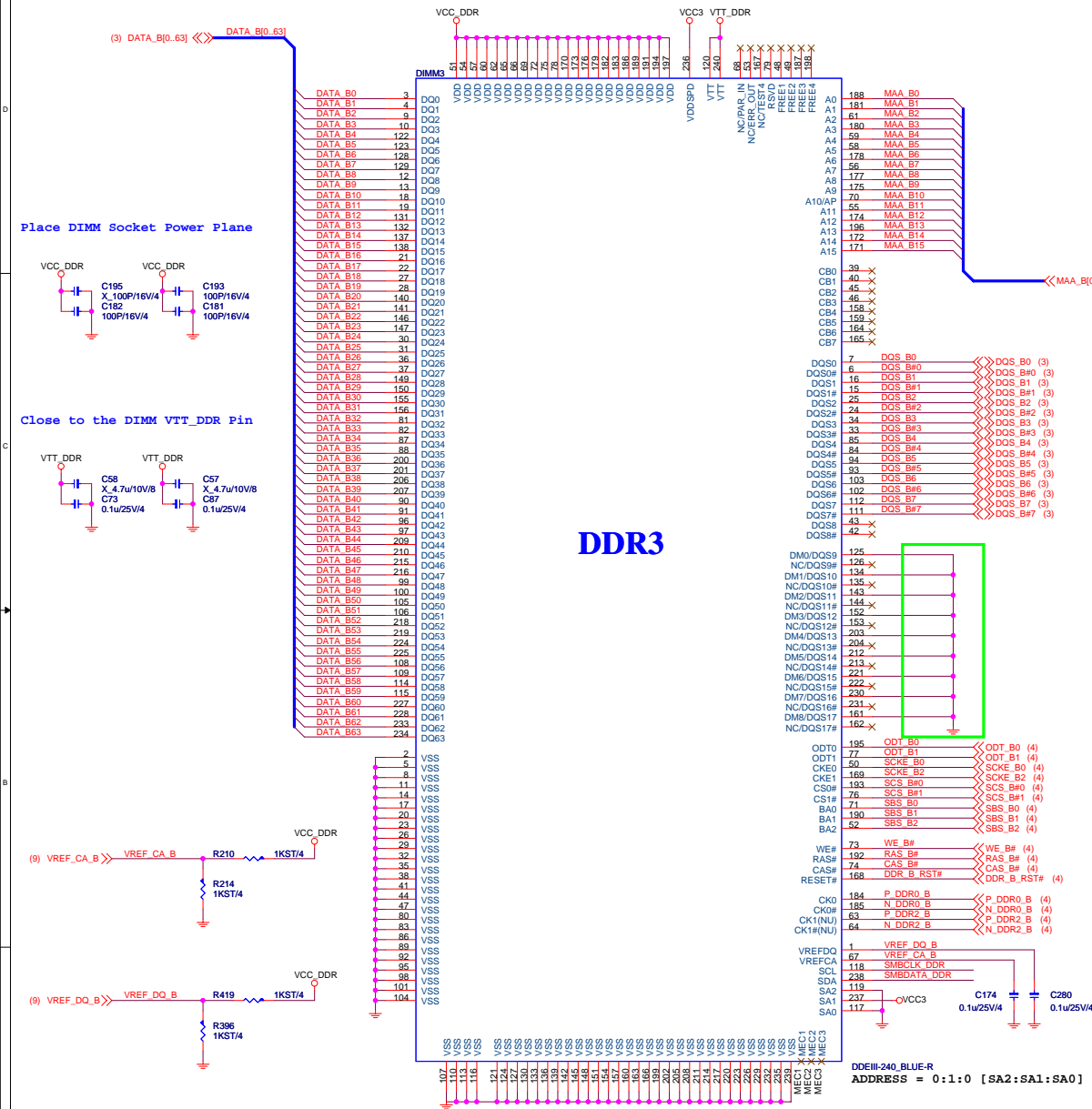
DIMM2 / CHANNEL A1



	MICRO-STAR INT'L CO.,LTD			
	MS-7520			
	Size Custom	Document Description DDR III DIMM 1 / DIMM 2		Rev 0
	Date: Thursday, March 13, 2008		Sheet 9 of 49	

DIMM3 / CHANNEL B0

DIMM4 / CHANNEL B1




Vref-DQ : Reference voltage for DQ0-DQ63, CB0-CB7 and PAR_IN. When in single ended mode used for DQS0-DQS7.

Vref-CA : Reference voltage for A0-A15, BA0-BA2, RAS#, CAS#, WE#, S0#, S01#, CKE0, CKE1, ODT0 and ODT1.

RESET#(Output) : A synchronously forces all registered output LOW when RESET# is LOW. This signal can be used during power up to ensure that CKE is LOW and DQs are High-Z.

SMBCLK_DDR SMBCLK_DDR (9,11)
SMBDATA_DDR SMBDATA_DDR (9,11)



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MS-7520

Size	Document Description	Rev
Custom	DDR III DIMM 3 / DIMM 4	0A

Date: Thursday, March 13, 2008 Sheet 10 of 49

DIMM5 / CHANNEL C0

Place DIMM Socket Power Plane

Close to the DIMM VTT_DDR Pin

DDR3

DIMM6 / CHANNEL C1

DDR3

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MS-7520

Size Custom Document Description **DDR III DIMM 5 / DIMM 6** Rev 0A

Date: Thursday, March 13, 2008 Sheet 11 of 49

DIMM5 / CHANNEL C0

DIMM6 / CHANNEL C1

DDR3

DDR3

**NON-SUPPORTED DIMM WARNING
CIRCUIT-- LED TURN ON**

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MS-7520

DDR III DIMM 5 / DIMM 6

Date: Thursday, March 13, 2008

Sheet 11 of 49

DIMM5 / CHANNEL C0

Place DIMM Socket Power Plane

Close to the DIMM VTT_DDR Pin

DDR3

DIMM6 / CHANNEL C1

DDR3

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Size Custom Document Description **DDR III DIMM 5 / DIMM 6** Rev 0A

Date: Thursday, March 13, 2008 Sheet 11 of 49

DIMM5 / CHANNEL C0

Place DIMM Socket Power Plane

Close to the DIMM VTT_DDR Pin

DDR3

DIMM6 / CHANNEL C1

DDR3

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MS-7520

Size Custom Document Description **DDR III DIMM 5 / DIMM 6** Rev 0A

Date: Thursday, March 13, 2008 Sheet 11 of 49

DIMM5 / CHANNEL C0

DIMM6 / CHANNEL C1

DDR3

DDR3

**NON-SUPPORTED DIMM WARNING
CIRCUIT-- LED TURN ON**

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MS-7520

DDR III DIMM 5 / DIMM 6

Date: Thursday, March 13, 2008

Sheet 11 of 49

DIMM5 / CHANNEL C0

DIMM6 / CHANNEL C1

DDR3

DDR3

**NON-SUPPORTED DIMM WARNING
CIRCUIT-- LED TURN ON**

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MICRO-STAR INT'L CO.,LTD

MS-7520

DDR III DIMM 5 / DIMM 6

Date: Thursday, March 13, 2008

Sheet 11 of 49

DIMM5 / CHANNEL C0

Place DIMM Socket Power Plane

Close to the DIMM VTT_DDR Pin

DDR3

DIMM6 / CHANNEL C1

DDR3

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MS-7520

Size Custom Document Description **DDR III DIMM 5 / DIMM 6** Rev 0A

Date: Thursday, March 13, 2008 Sheet 11 of 49

DIMM5 / CHANNEL C0

Place DIMM Socket Power Plane

Close to the DIMM VTT_DDR Pin

DDR3

DIMM6 / CHANNEL C1

DDR3

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MS-7520

Size Custom Document Description **DDR III DIMM 5 / DIMM 6** Rev 0A

Date: Thursday, March 13, 2008 Sheet 11 of 49

DIMM5 / CHANNEL C0

DIMM6 / CHANNEL C1

DDR3

DDR3

**NON-SUPPORTED DIMM WARNING
CIRCUIT-- LED TURN ON**

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MS-7520

DDR III DIMM 5 / DIMM 6

Date: Thursday, March 13, 2008

Sheet 11 of 49

DIMM5 / CHANNEL C0

DIMM6 / CHANNEL C1

DDR3

DDR3

**NON-SUPPORTED DIMM WARNING
CIRCUIT-- LED TURN ON**

MSI

MICRO-STAR INT'L CO.,LTD

MS-7520

DDR III DIMM 5 / DIMM 6

Date: Thursday, March 13, 2008

Sheet 11 of 49

DIMM5 / CHANNEL C0

Place DIMM Socket Power Plane

Close to the DIMM VTT_DDR Pin

DDR3

DIMM6 / CHANNEL C1

DDR3

MSI

MICRO-STAR INT'L CO.,LTD

MS-7520

Size Custom Document Description **DDR III DIMM 5 / DIMM 6** Rev 0A

Date: Thursday, March 13, 2008 Sheet 11 of 49

DIMM5 / CHANNEL C0

Place DIMM Socket Power Plane

Close to the DIMM VTT_DDR Pin

DDR3

DIMM6 / CHANNEL C1

DDR3

MSI

MICRO-STAR INT'L CO.,LTD

MS-7520

Size Custom Document Description **DDR III DIMM 5 / DIMM 6** Rev 0A

Date: Thursday, March 13, 2008 Sheet 11 of 49

DIMM5 / CHANNEL C0

DIMM6 / CHANNEL C1

DDR3

DDR3

**NON-SUPPORTED DIMM WARNING
CIRCUIT-- LED TURN ON**

MSI

MICRO-STAR INT'L CO.,LTD

MS-7520

DDR III DIMM 5 / DIMM 6

Date: Thursday, March 13, 2008

Sheet 11 of 49

VRM_EN

Voltage regulator module enable:

'0' = CSI PLL uses on-die voltage regulator (normal mode).

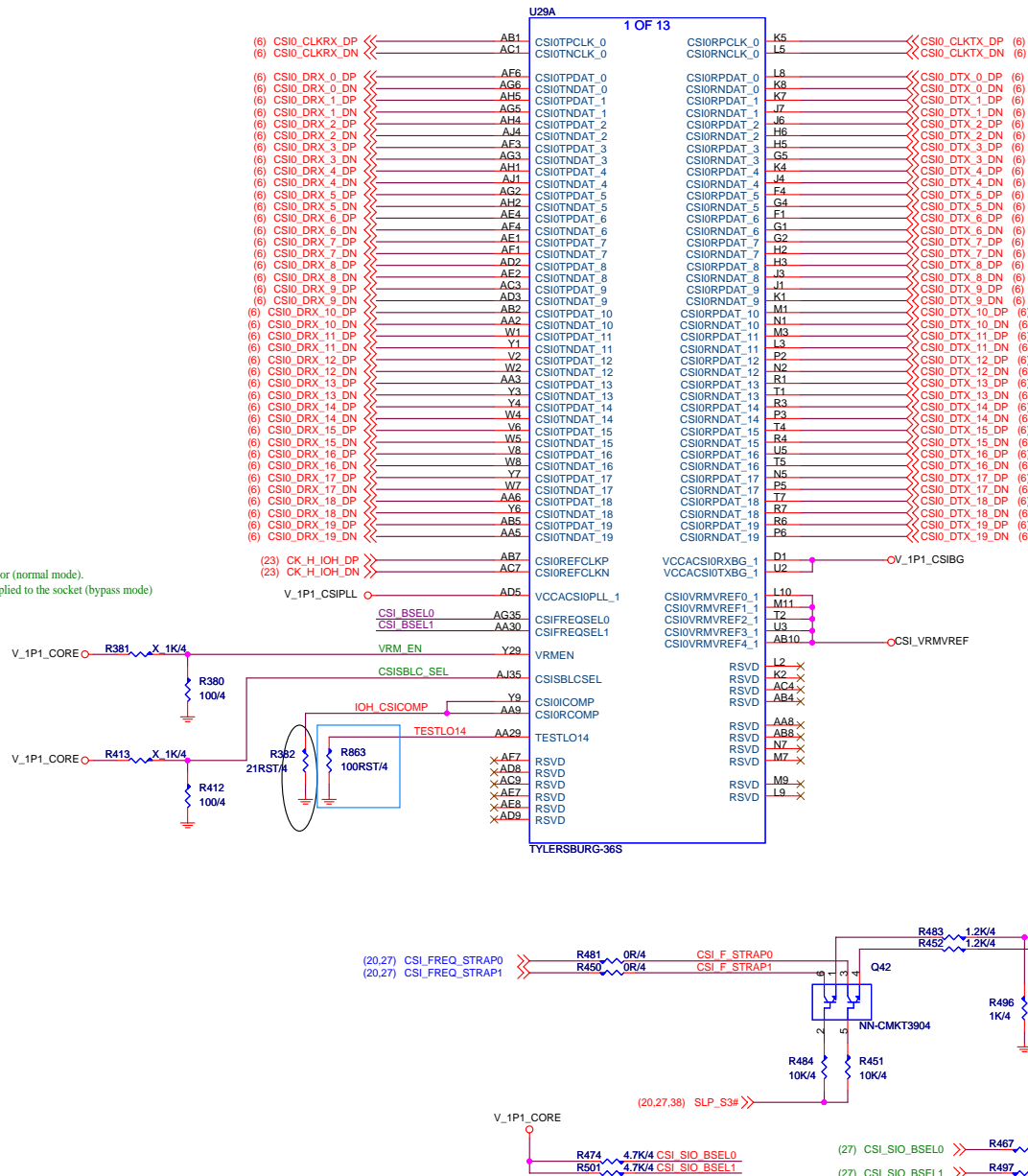
'1' = CSI PLL uses LC-filtered power supplied to the socket (bypass mode)

CSISBLC_SEL

CSI SB/ LC PLL select.

0 = CSI LC PLL (default)

1 = CSI SB PLL

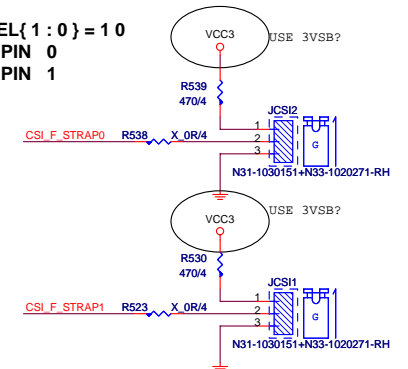


IOH_CSI_FREQUENCY SELECTION	
SEL{1:0}	CSI FREQUENCY (GT / S)
00	4.8
01	5.867
10	6.4 (DEFAULT)
11	RSVD

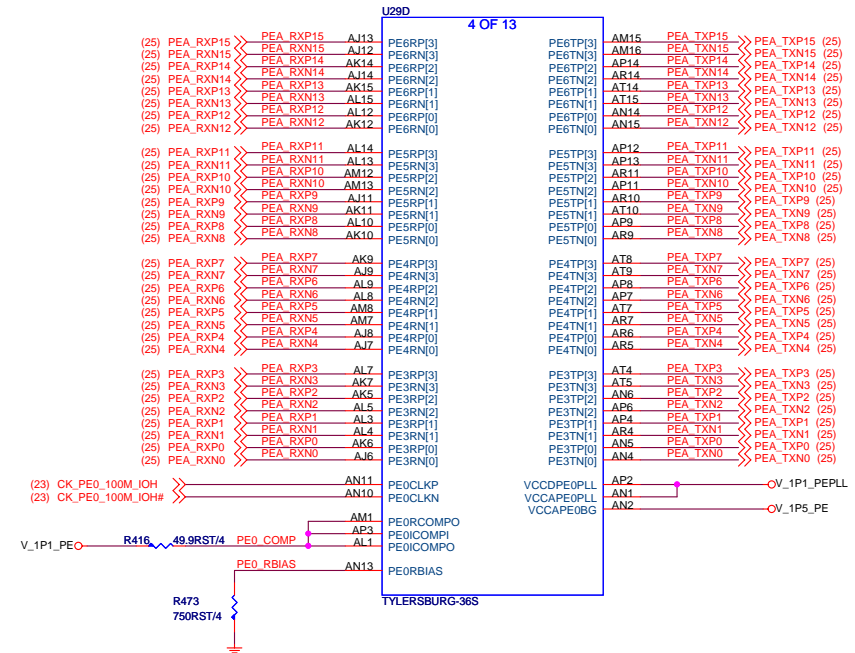
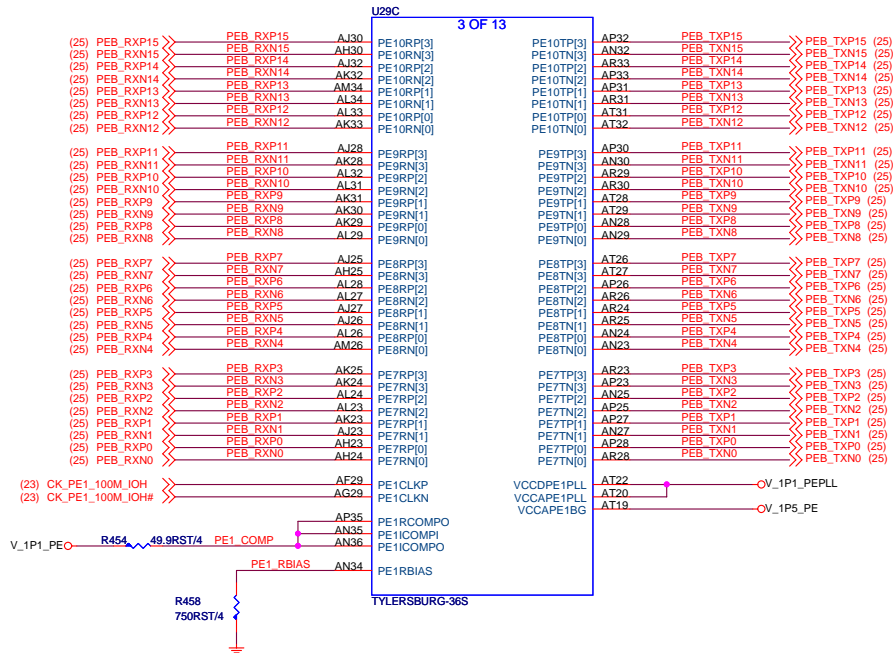
Default SEL{1:0} = 10

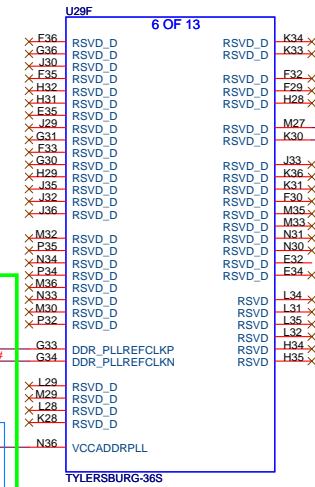
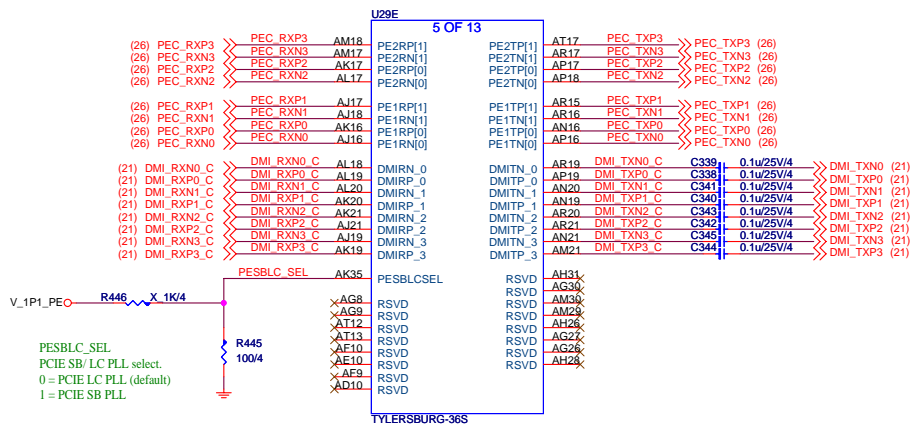
JCSI2 2-3 PIN 0

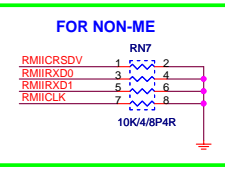
JCSI1 1-2 PIN 1

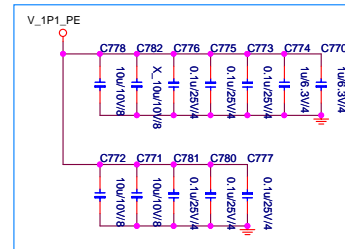
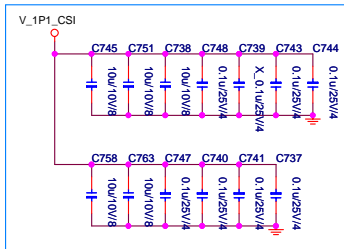
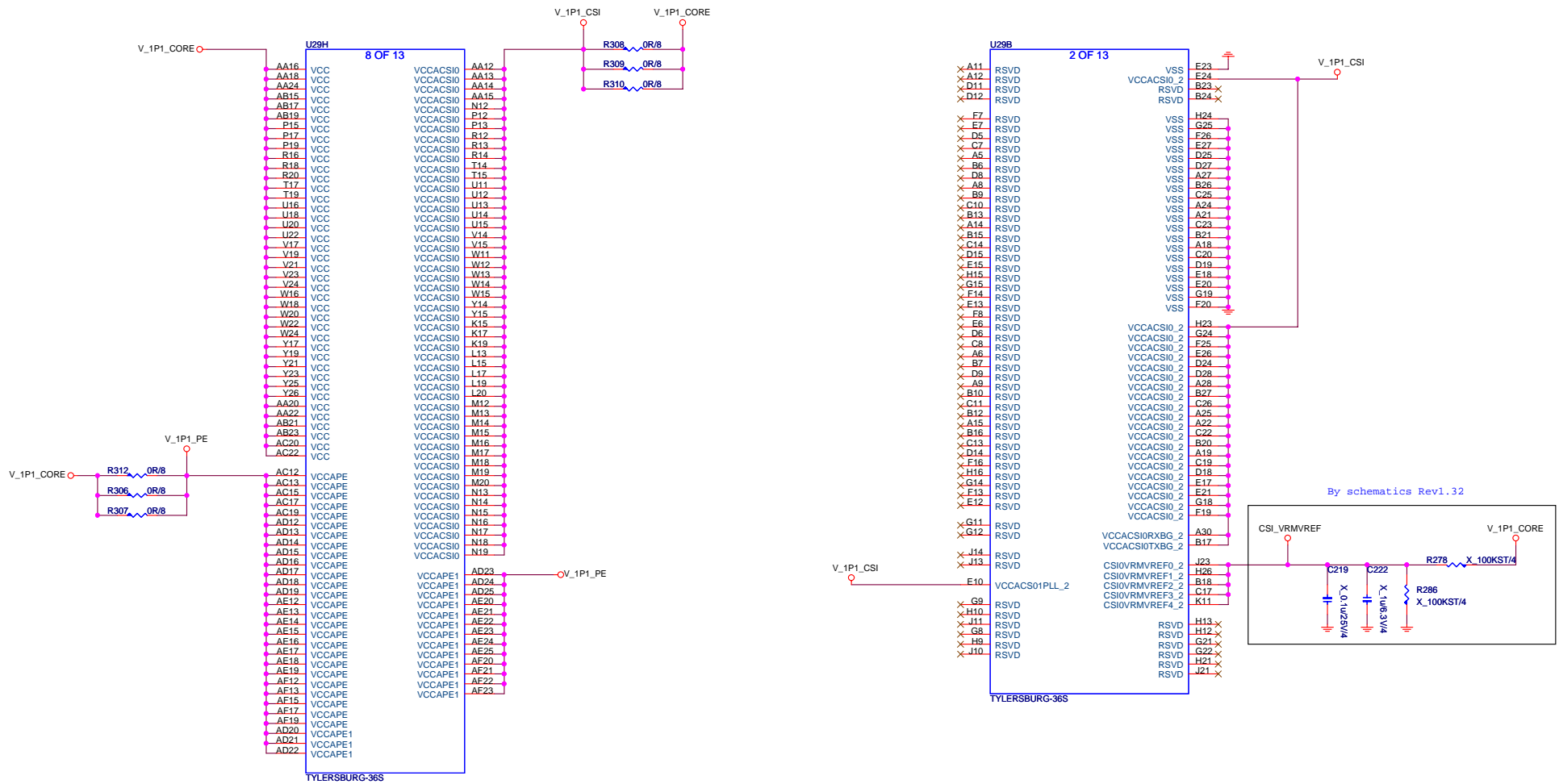


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MS-7520			
Size	Document Description	Rev	
Custom	IOH 36S-CSI	0A	
Date:	Thursday, March 13, 2008	Sheet	12 of 49







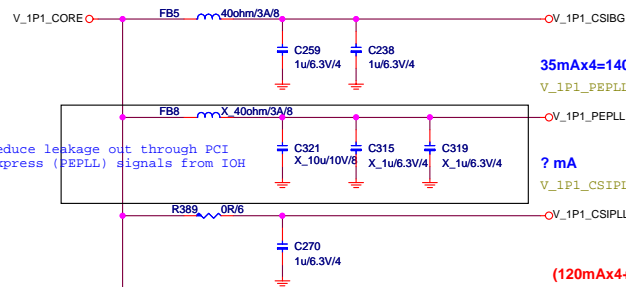


V_1P1_CORE REPLACE WITH V_1P1_VCCA

0.7A???

10mA \times 2=20mA

V_1P1_CSIBG = CSIBG_RX+CSIBG_TX



35mA \times 4=140mA

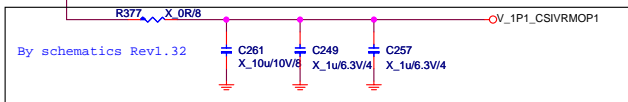
V_1P1_PEPLL = PEPLLA+PEPLLD

? mA

V_1P1_CSIPLL = CSI_PLL

(120mA \times 4+60mA)??=0.54A ?????

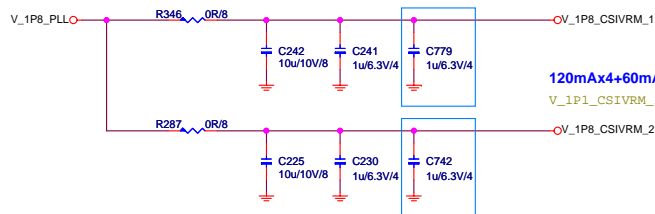
V_1P1_CSIVRMOP1 = CSIVRMOP_RX[1:4]+CSIVRMOP_TX1



1.08A

120mA \times 4+60mA=0.54A

V_1P1_CSIVRM_1 = CSIVRM_RX_1+CSIVRM1_TX_1



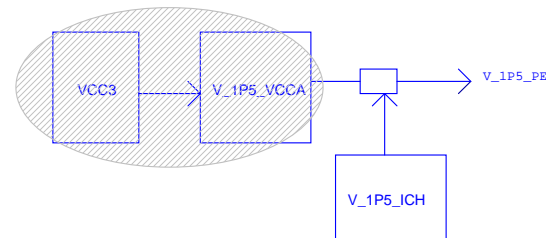
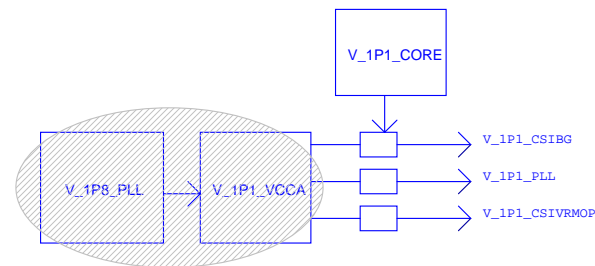
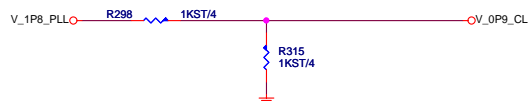
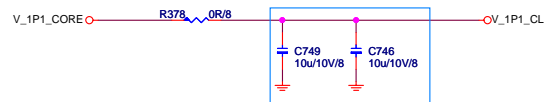
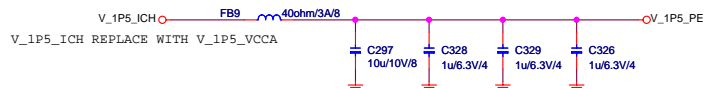
120mA \times 4+60mA=0.54A

V_1P1_CSIVRM_2 = CSIVRM_RX_2+CSIVRM1_TX_2

186.3mA+?

92mA \times 2+1.15mA \times 2+=186.3mA+?

V_1P5_PE = PEVRM+PEBG0+PEBG1+VCCTS

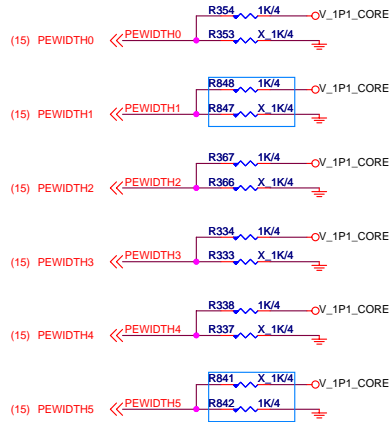


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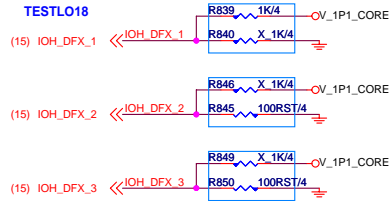
MS-7520

Size	Document Description	Rev
Custom	IOH 36S-ANALOG FILTER	0A
Date:	Thursday, March 13, 2008	Sheet 18 of 49

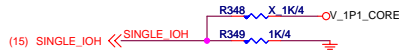
PEWIDTH0~5
PCIE Link Width Select
"111011" = 2x16
"101111" = 4x8
"011111" = Wait On Bios



IOH_DFX_2 , 3]
DDR frequency selection pins:
DDR[FREQ]3:2 as DDR frequency selection defined as:
"00" = 133MHz input, 200MHz core
"01" = 100 MHz input, 200MHz core
"10" = RSVD
"11" = RSVD



SINGLE_IOH
Used for dual TBG IOH selection:
"0": IOH is not connected to another IOH on some CSI link (default)
"1": IOH is connected to another IOH on some CSI link

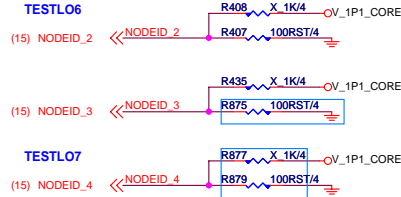


CL_CLK_SRC
Used for ME default clock source:
"1": PLL (default)
"0": Ring Oscillator (back-up)

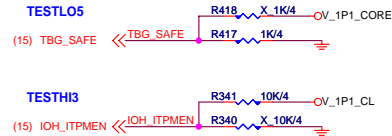
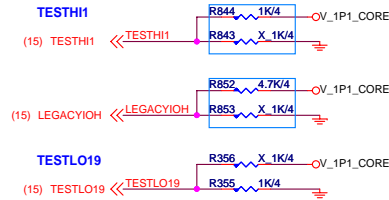


NON-ME FUNCTION ?

NODEID_3_TBG
For dual TBG IOH configuration,
it indicates which CSI port is connected
to the other IOH.
"0": CSI0
"1": CSI1



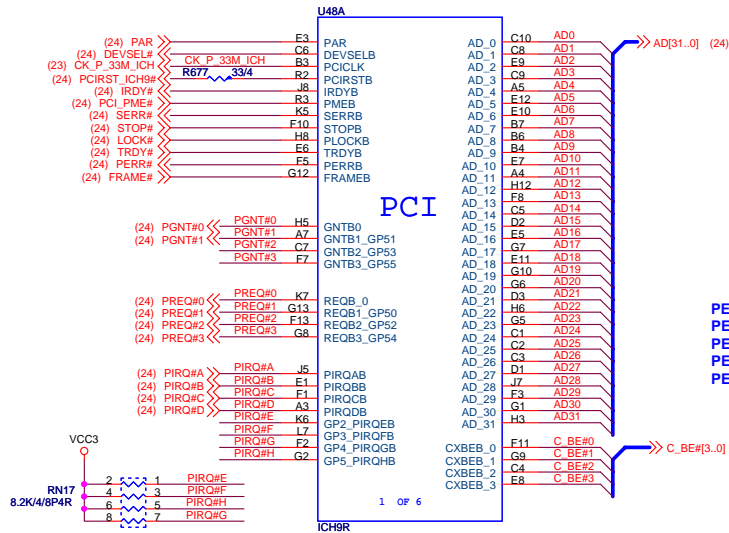
LEGACYIOH
Used to determine legacy or non-legacy selection:
"1": Legacy IOH
"0": Non-legacy IOH



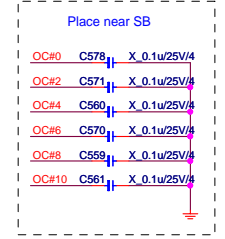
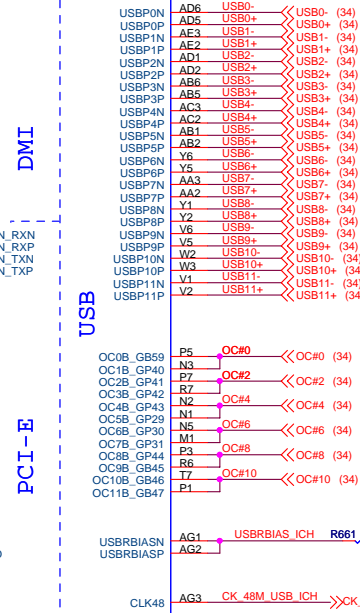
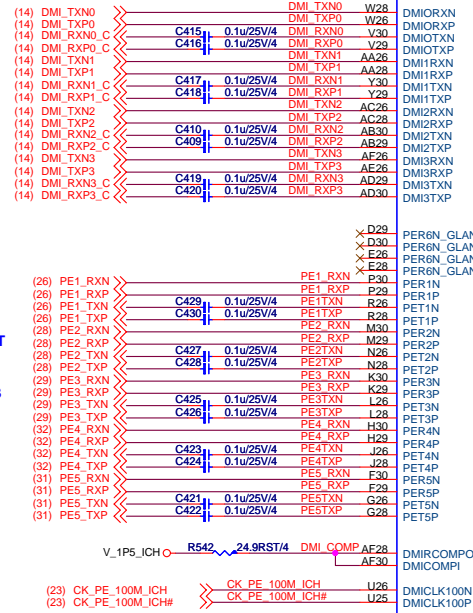
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MS-7520

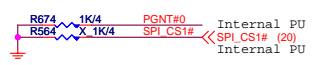
Size Custom	Document Description IOH 36S-STRAP	Rev 0A
Date: Thursday, March 13, 2008	Sheet 19 of 49	



PE1 : X1 SLOT
PE2 : LAN1
PE3 : LAN2
PE4 : JMB363
PE5 : JMB381



SB STRAPPING RESISTOR



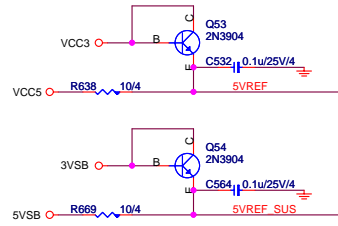
BOOT SELECT STRAPS		
BOOT DEVICE	GNT#0	SPI_CS1#
LPC	1	1
SPI	0	1
PCI	1	0



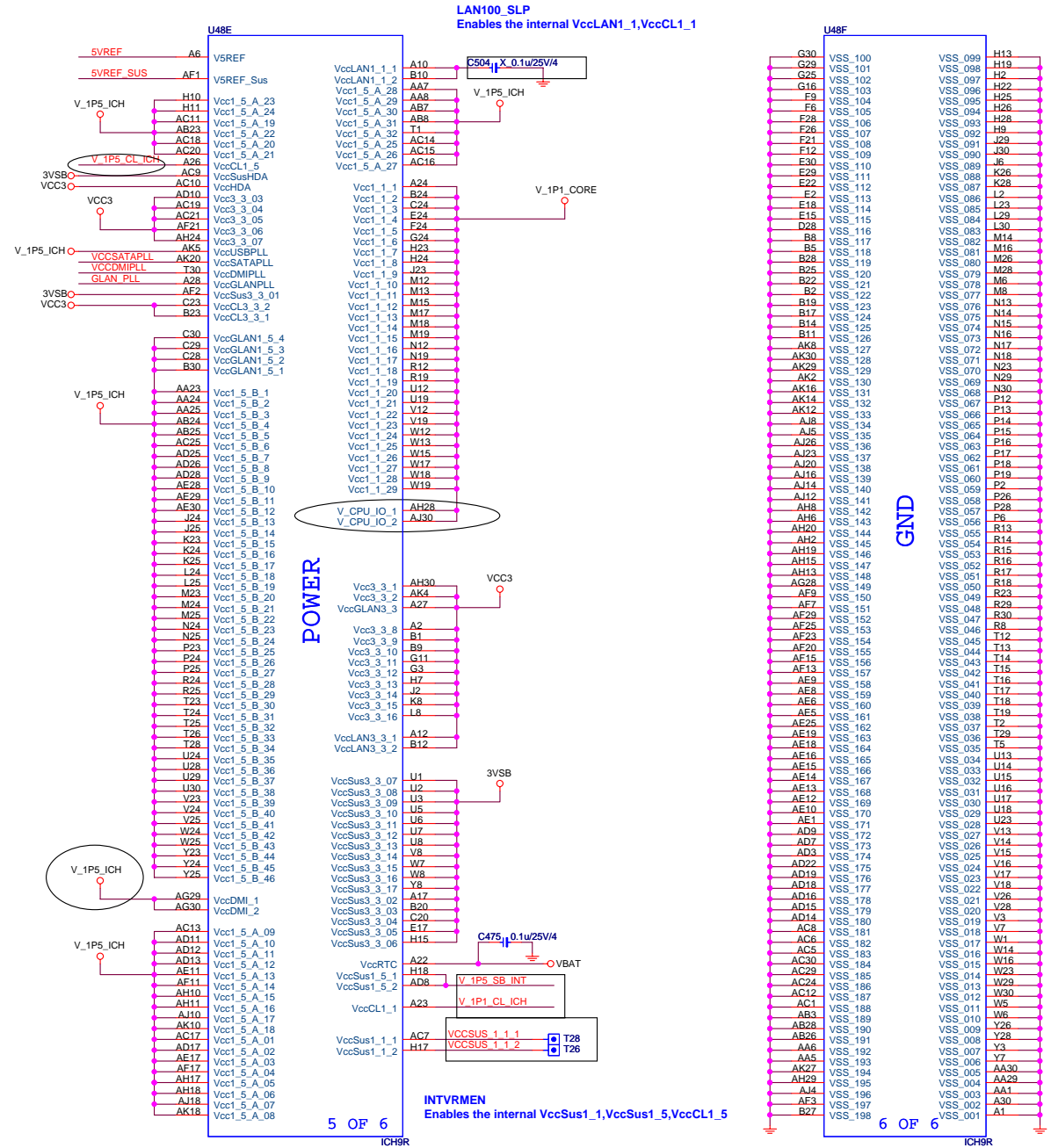
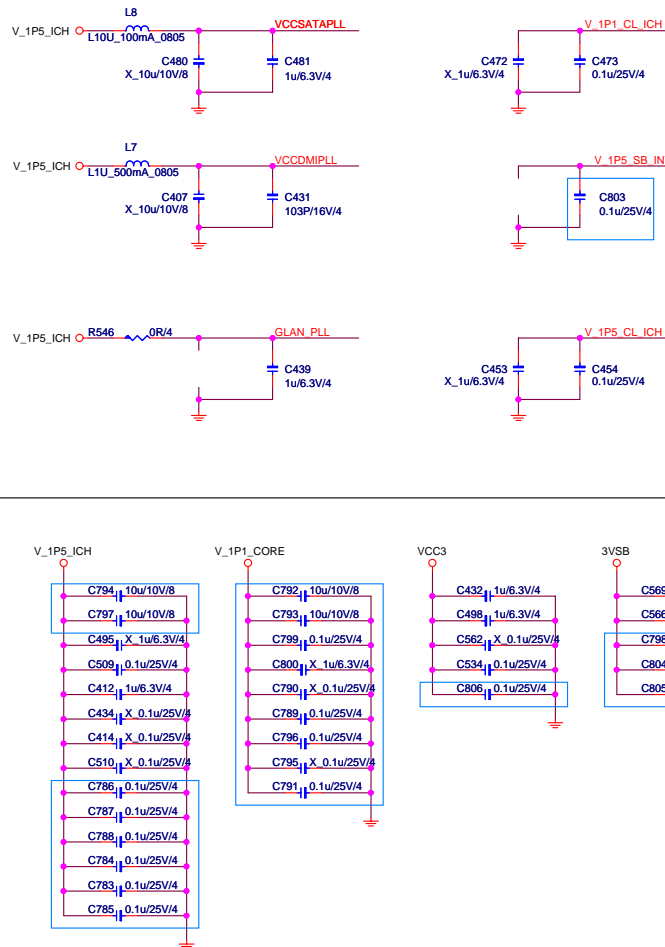
SIGNAL	H	L	DES.
GNT3	DIS	EN	A16 OVERRIDE
GNT2	N/A	SET BIT	PCIE PORT CONFIG 2 BIT 0 (5-6)
GNT1	DC	AC	DMI AC/DC MODE 0 : AC 1 : DC

MICRO-STAR INT'L CO.,LTD
MS-7520
Size Custom Document Description **ICH9_PCI, USB, DMI, PCIE x1** Rev 0A
Date: Thursday, March 13, 2008 Sheet 21 of 49

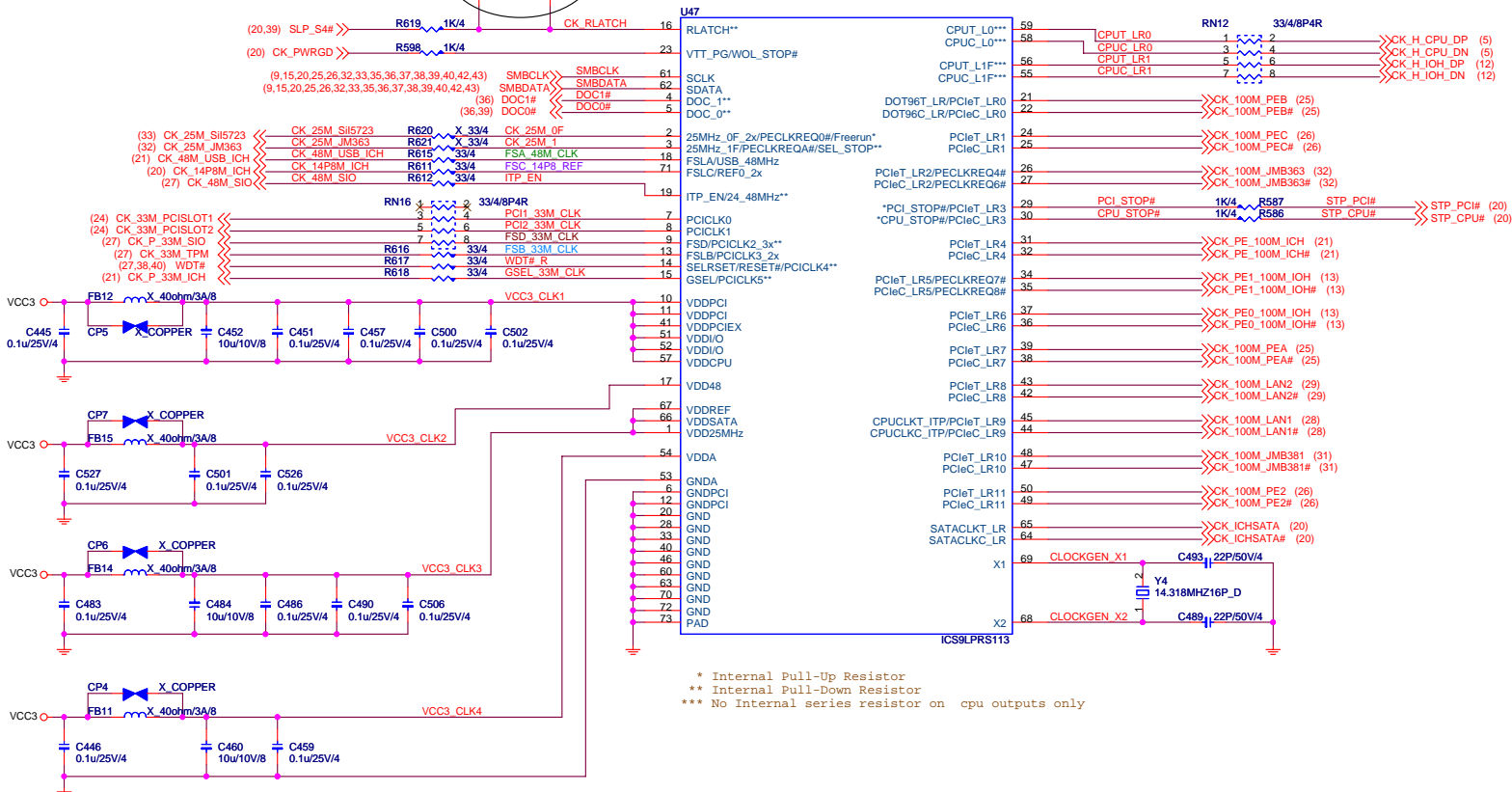
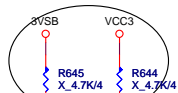
5VREF & 5VREF_SUS Sequencing Circuit



SB POWER



Clock Gen ICS9LPRS110A

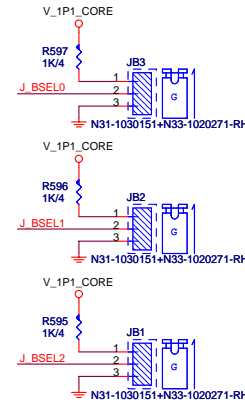
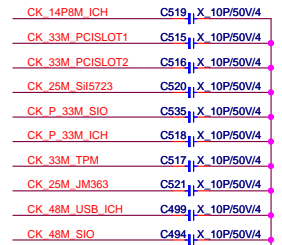
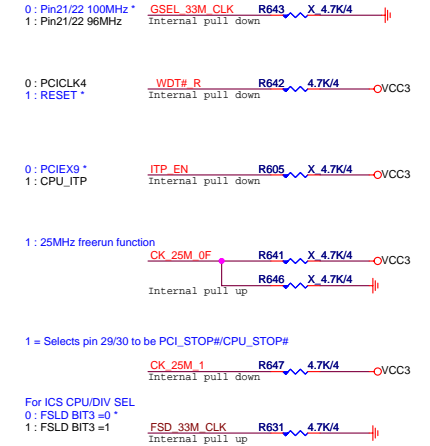


Default 0 0 1 133 MHz
JB3 1-2 PIN 1
JB2 2-3 PIN 0
JB1 2-3 PIN 0

BSEL	TABLE
2 1 0	FSB FREQUENCY
0 0 0	266 MHz
0 0 1	133 MHz (default)
0 1 0	200 MHz
0 1 1	166 MHz
1 0 0	333 MHz
1 0 1	100 MHZ
1 1 0	400 MHZ
1 1 1	200 MHZ

FSA 48M CLK R627 1K/4 J BSEL0
FSB 33M CLK R632 1K/4 J BSEL1
FSC 14P8 REF R625 1K/4 J BSEL2

CLOCK GEN STRAPING



MICRO-STAR INT'L CO.,LTD			
MS-7520			
Size	Document Description	Rev	0A
Custom	Clock Gen ICS9LPRS113		
Date:	Thursday, March 13, 2008	Sheet	23 of 49

PCI SLOT 2 (PCI VER: 2.2 COMPLY)

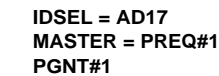
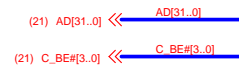
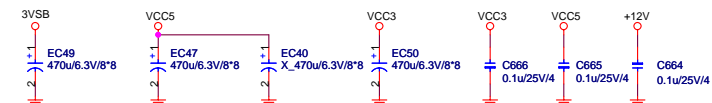
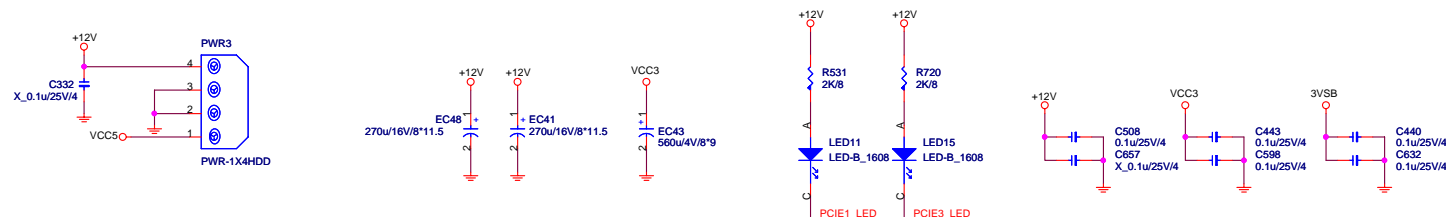
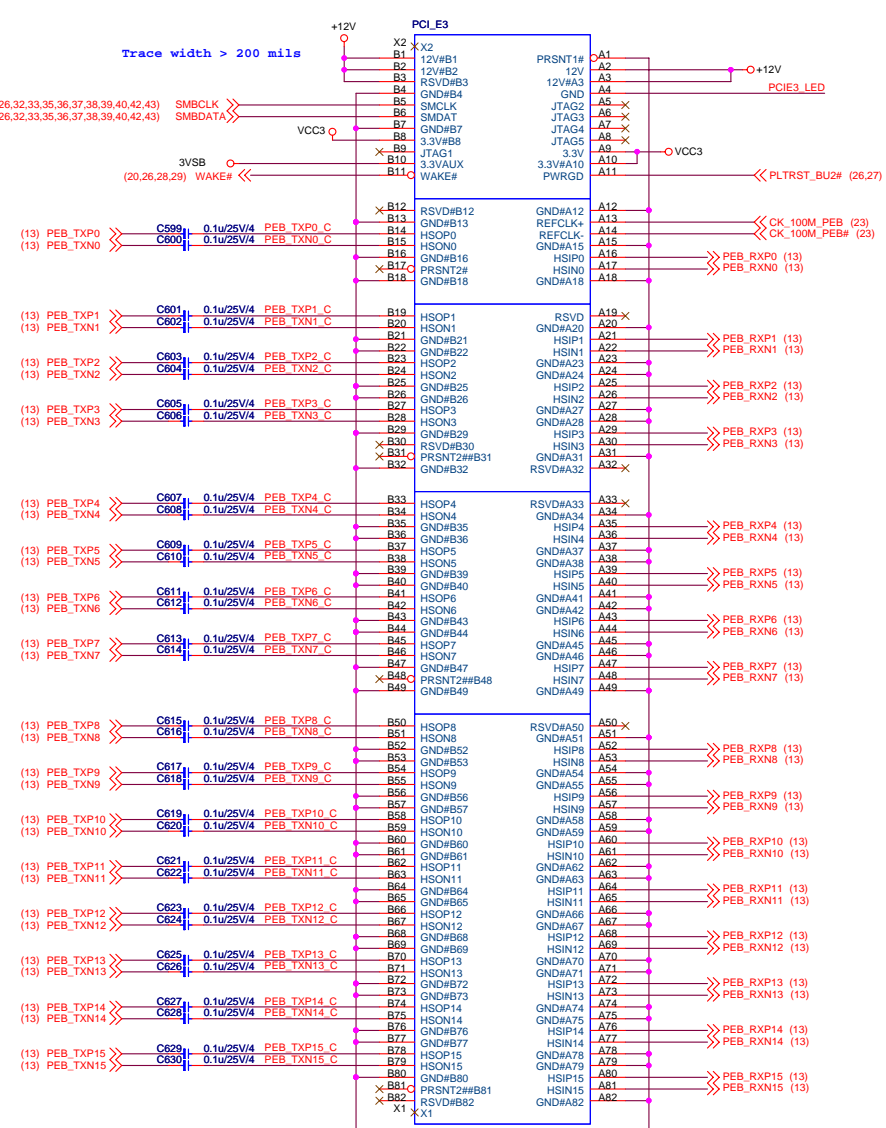
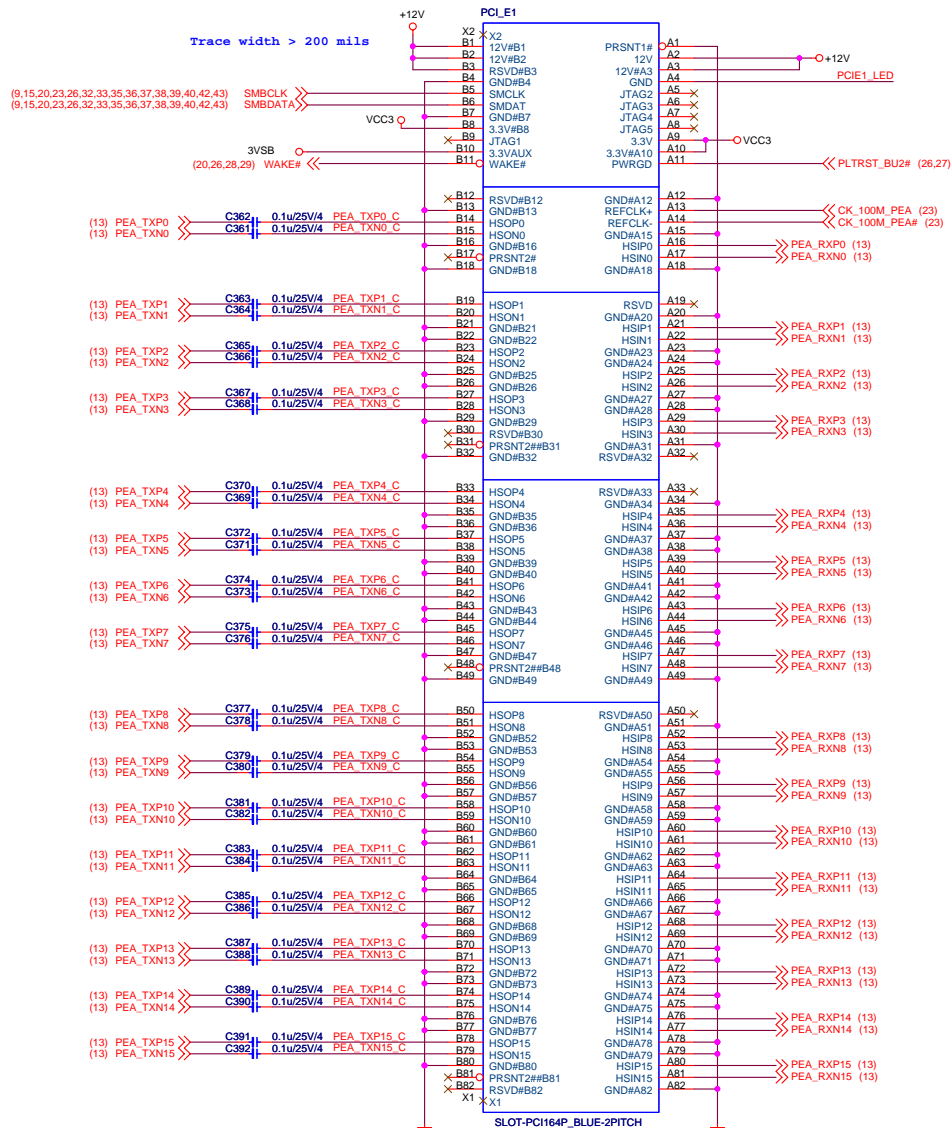


Figure 10 shows the pin connections for the R759 module. The diagram is divided into two main sections, each connected to a VCC3 supply. The top section includes signals like DEVSEL#, TRDY#, IRDY#, FRAME#, SERR#, PERR#, LOCK#, STOP#, REQ#64, ACK#64, and PCI_PME#. The bottom section includes signals like PREQ#0-3, PIQ#C-A, and R759. Each signal is connected to a specific pin on the module, with some pins having multiple connections (e.g., R681, R626, R614, R667, R791, R792, R759).

**MS-7520**

Size Custom	Document Description PCISLOT1, 2	Rev 0A
Date: Thursday, March 13, 2008		Sheet 24 of 49

PCI Express X16 SLOT1,2

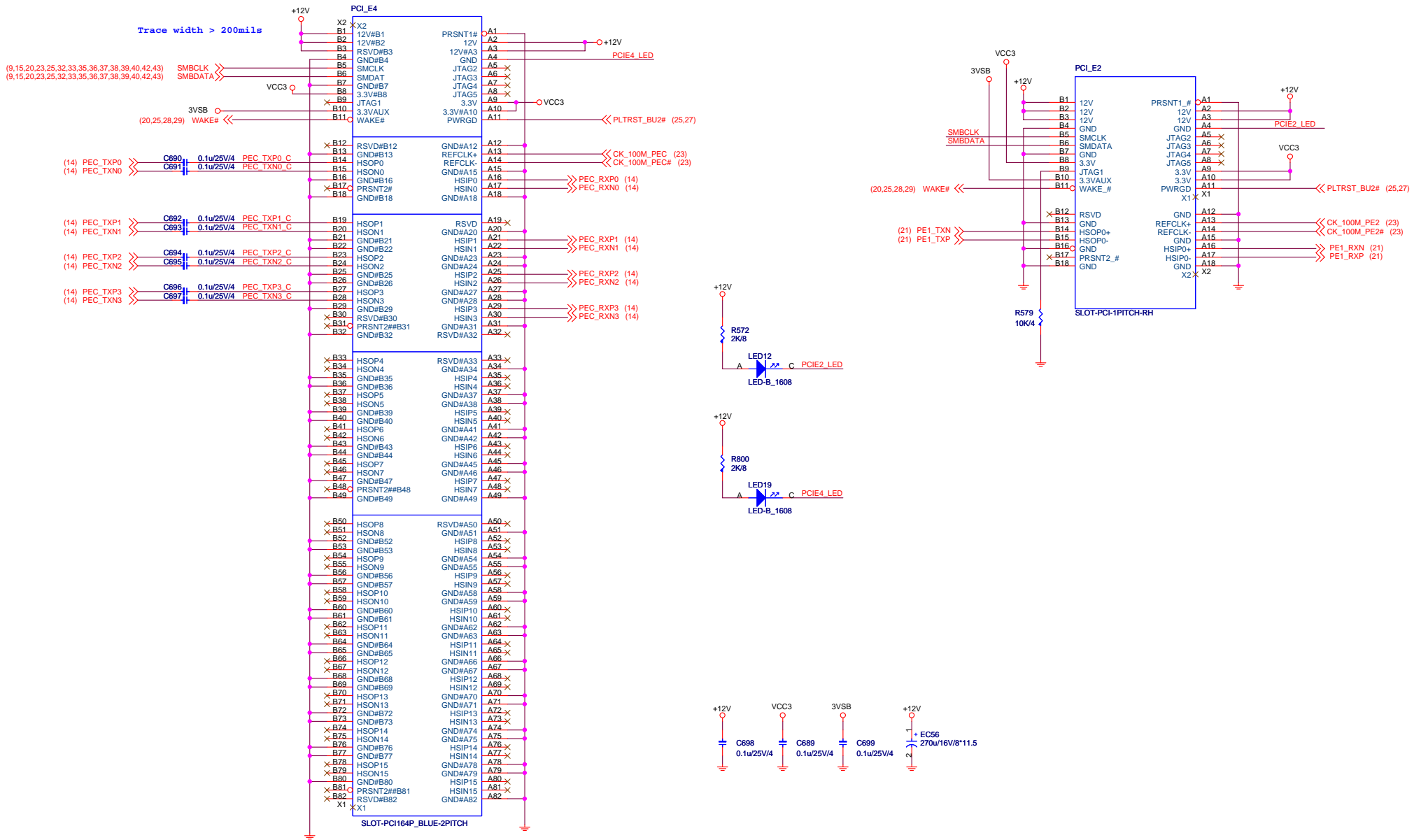


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MS-7520

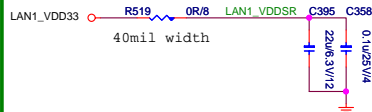
Size	Document Description	Rev
Custom	PCI-E X16 SLOT1, 2	0A
Date: Thursday, March 13, 2008	Sheet 25 of 49	

PCI_Express X4 Slot

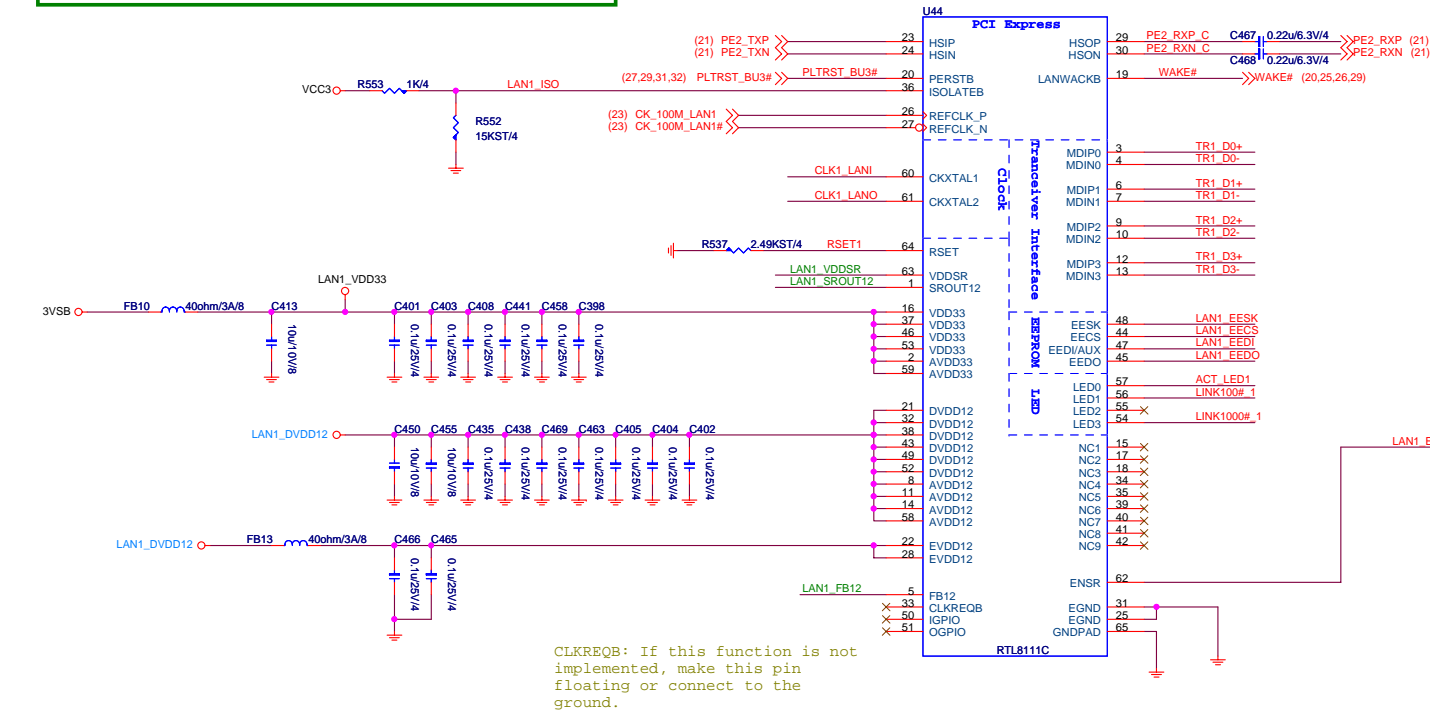


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MS-7520			
Size	Document Description	Rev	
Custom	PCI-E X4/X1 SLOT	0A	
Date:	Thursday, March 13, 2008	Sheet	26 of 49

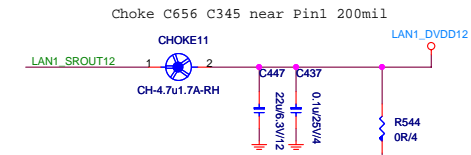
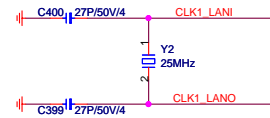
For the power pin of the switching regulator,
Disable switching regulator: Remove R27, C20, C21



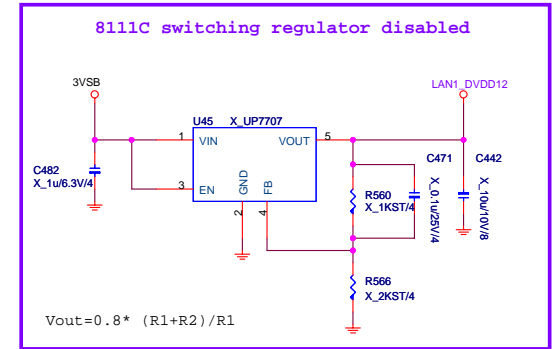
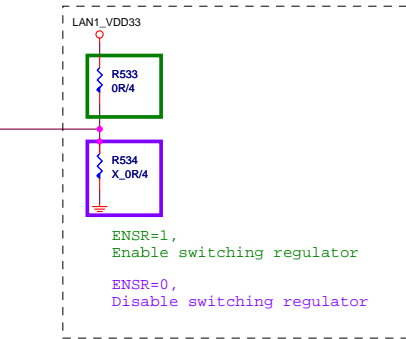
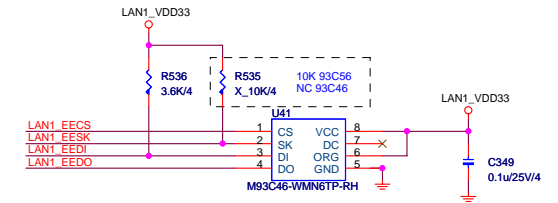
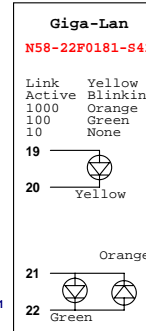
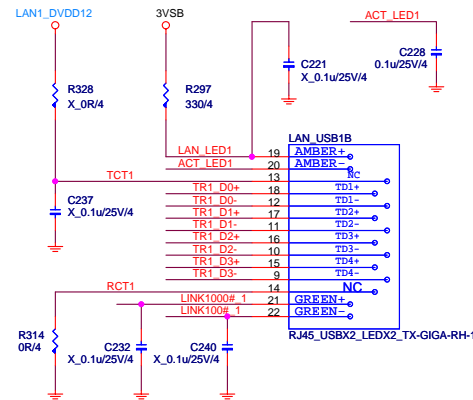
C657 C346 near Pin63 200mil, C346 must be nearly Pin63



CLKREQB: If this function is not implemented, make this pin floating or connect to the ground.

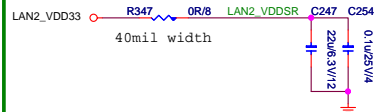


"FB12": A trace front CHOKE to RTL8111C pin5

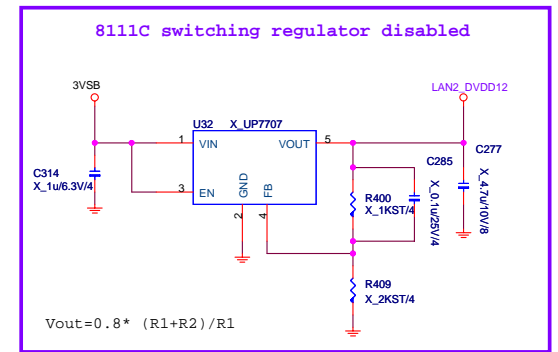
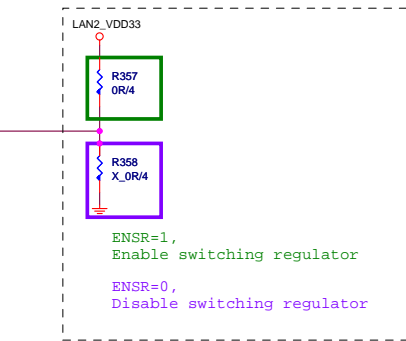
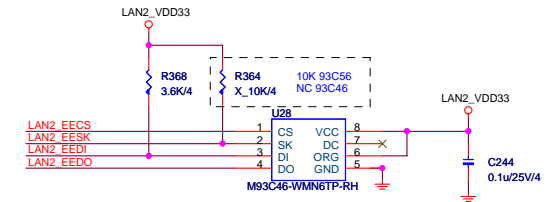
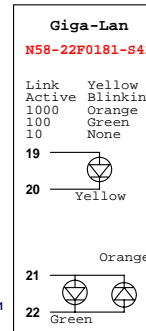
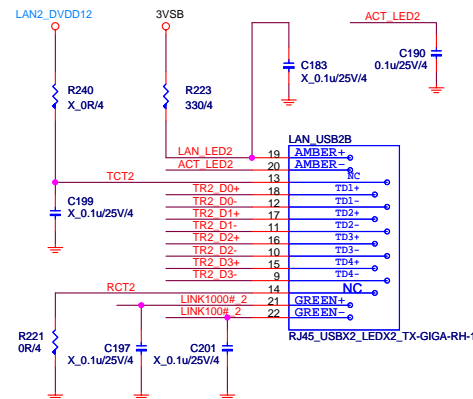
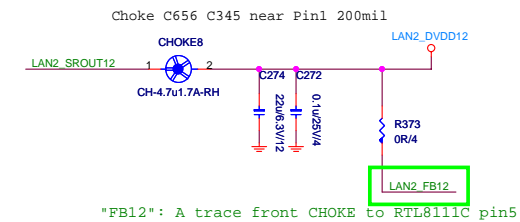
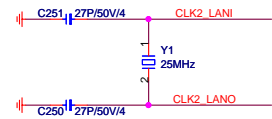
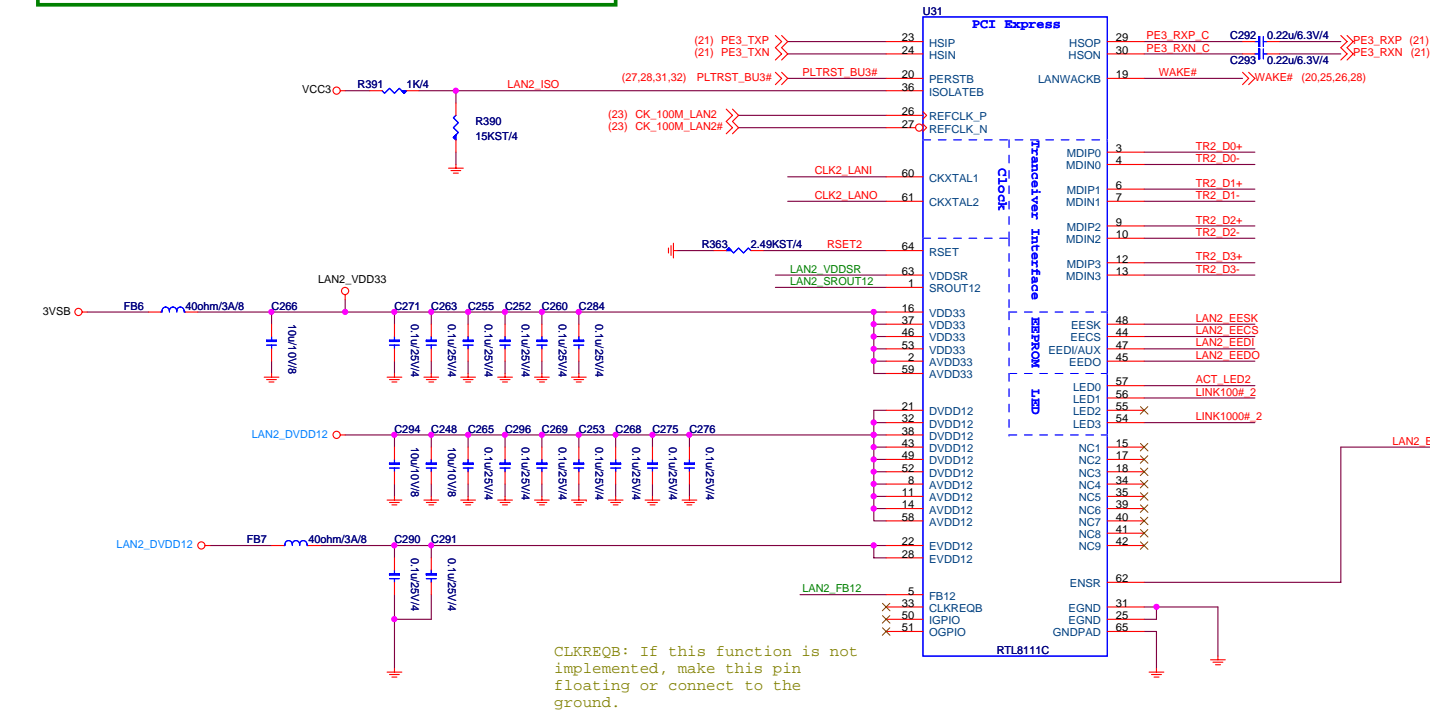


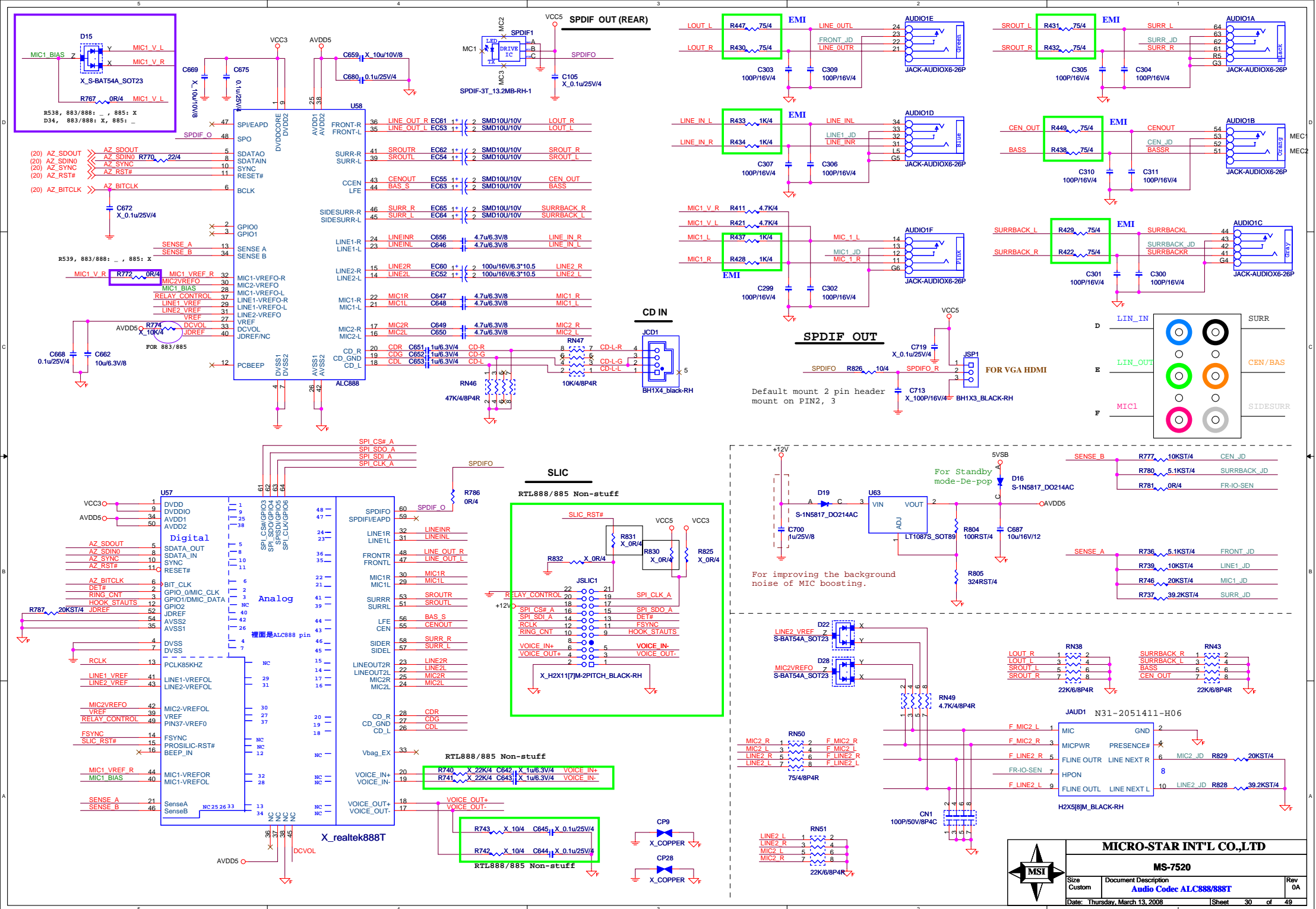
MICRO-STAR INT'L CO.,LTD		
MS-7520		
Size	Document Description	Rev
Custom	LAN1 - RTL8111C	0A
Date: Thursday, March 13, 2008	Sheet 28 of 49	

For the power pin of the switching regulator,
Disable switching regulator: Remove R27, C20, C21

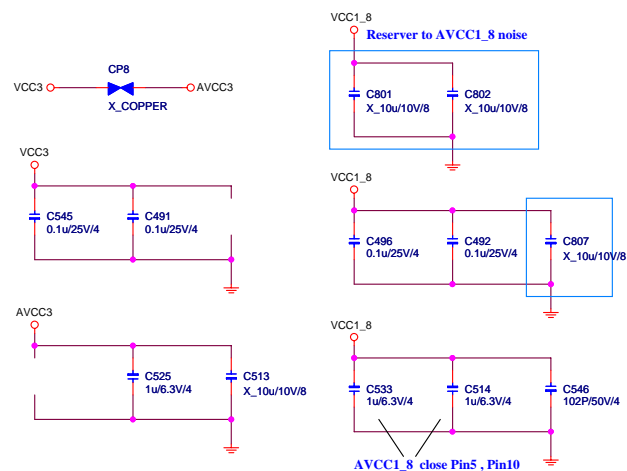
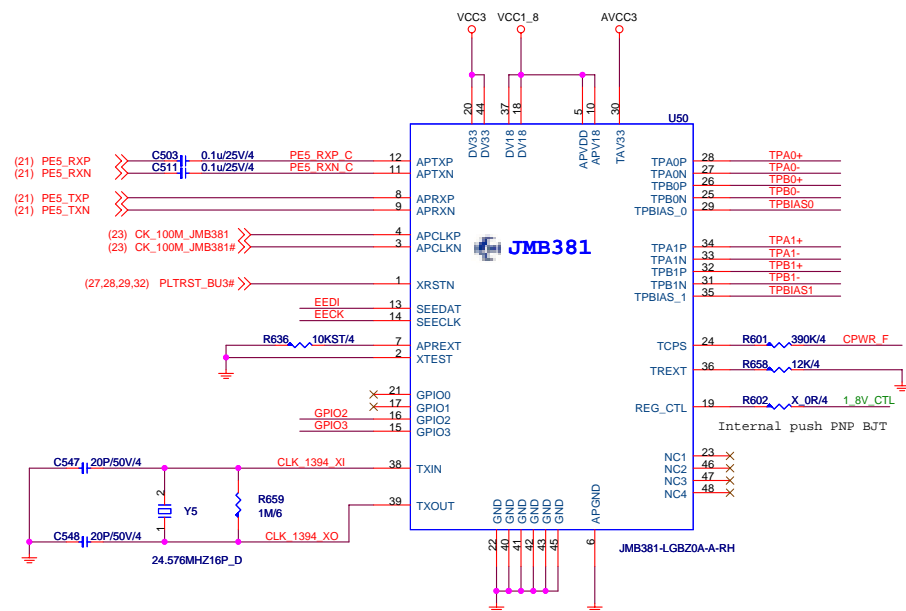


C657 C346 near Pin63 200mil, C346 must be nearly Pin63

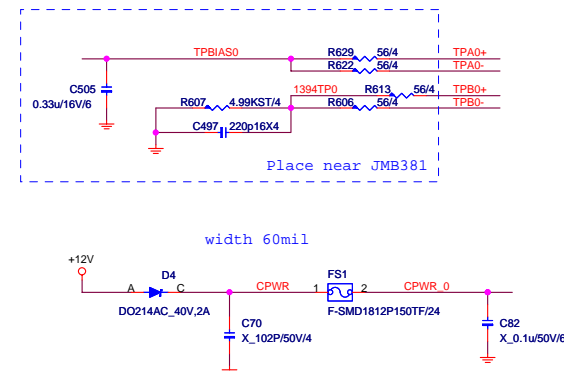




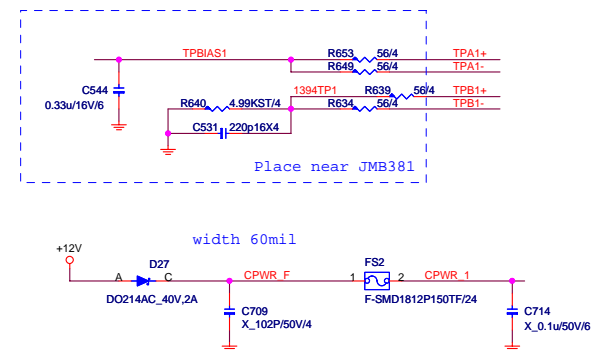
1394 CONTROLLER



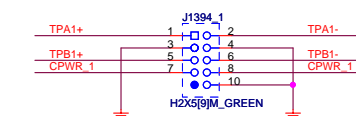
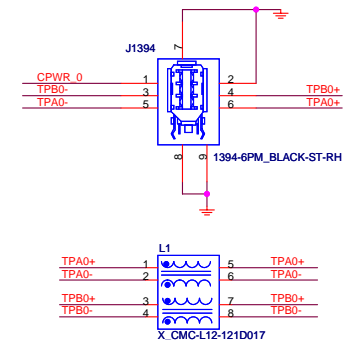
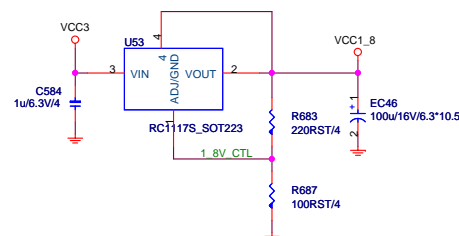
Rear 1394 port



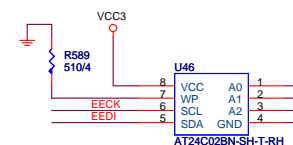
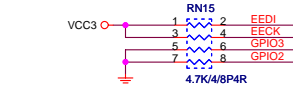
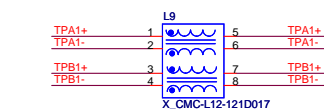
Front 1394 pin header



A1117 CO-LAY SOT223 (TO_261) PNP BJT



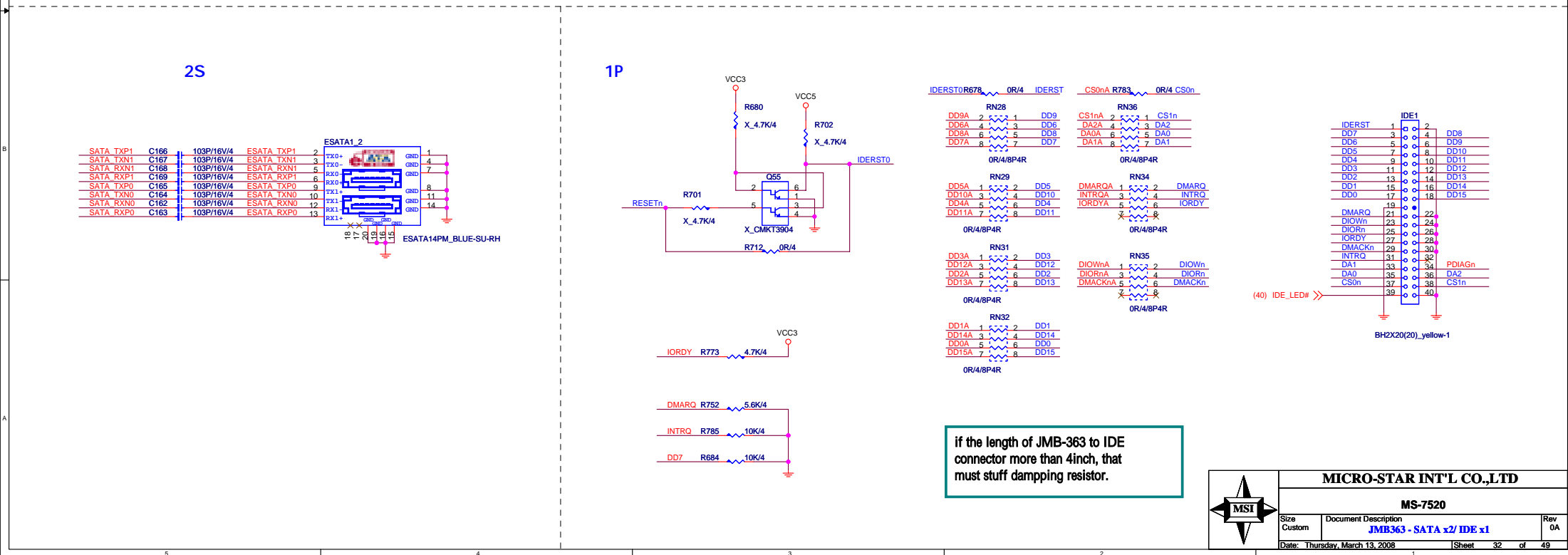
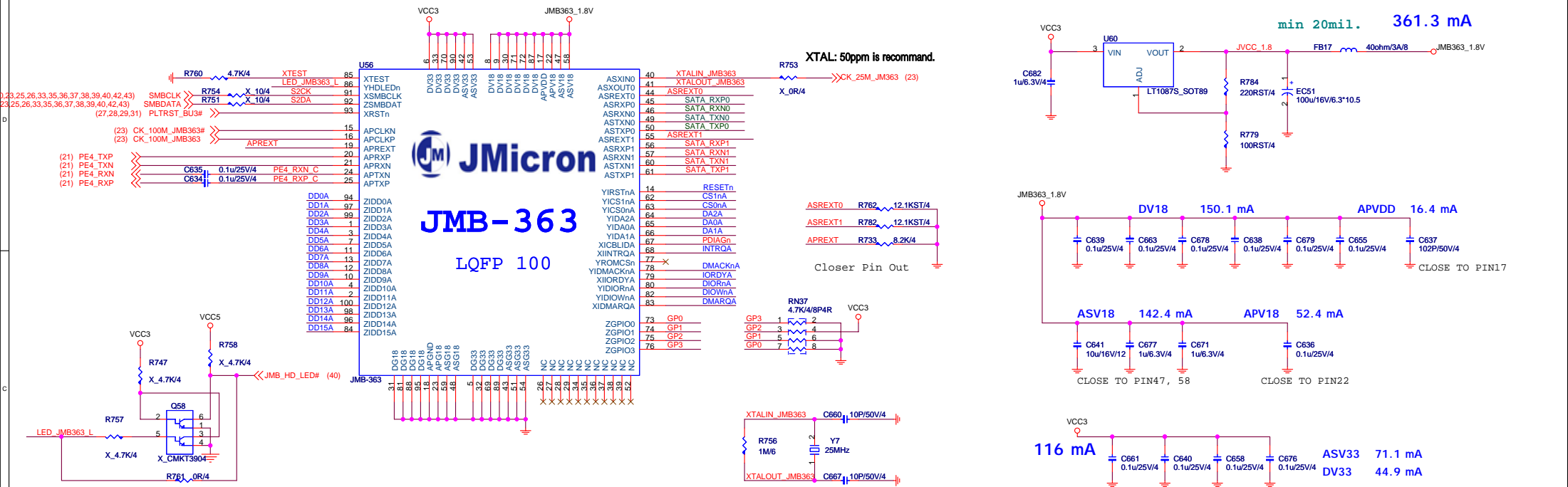
For Intel 1394 pinheader

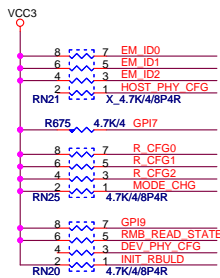


MICRO-STAR INT'L CO.,LTD

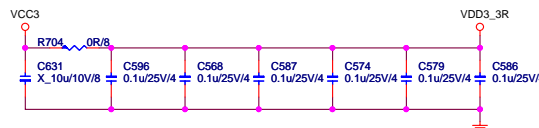
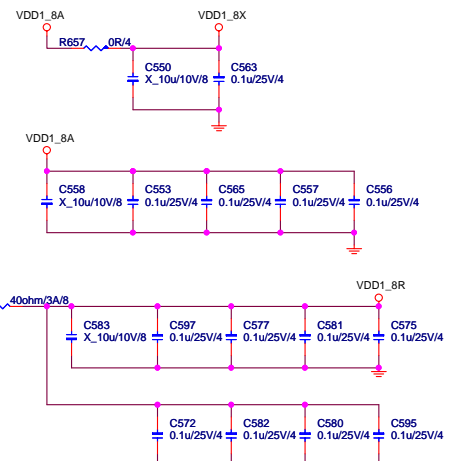
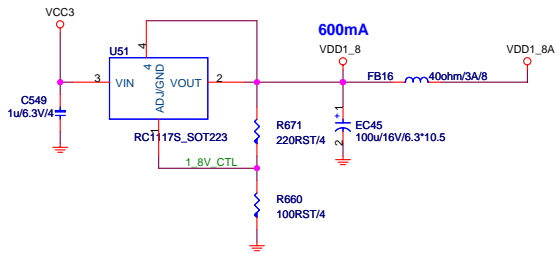
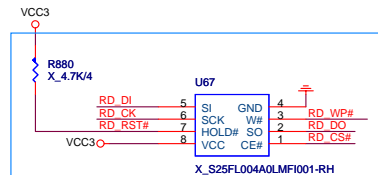
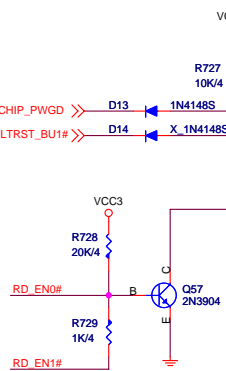
MS-7520

Size Custom	Document Description 1394 Controller - JMB381	Rev 0A
Date: Thursday, March 13, 2008		Sheet 31 of 49



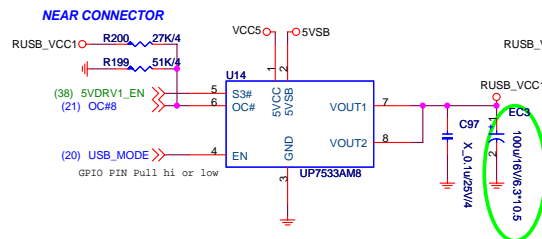


GPI7 EASY BACKUP
CFG 1:0
0 0 BIG
0 1 JBOD
1 0 FAST(RAID0)
1 1 SAFE(RAID1)
CFG 3 : MODE CHANGE

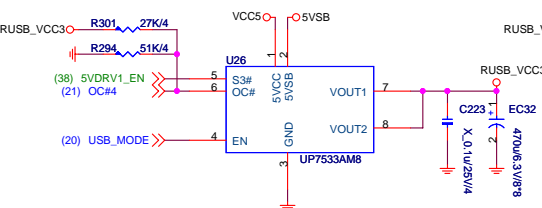


MICRO-STAR INT'L CO.,LTD			
MS-7520			
Size	Document Description	Rev	
Custom	SI5723 - RAID SATA x2	0A	
Date:	Thursday, March 13, 2008	Sheet	33 of 49

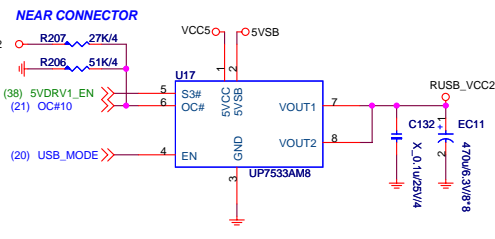
USB POWER FOR PORT 0,1



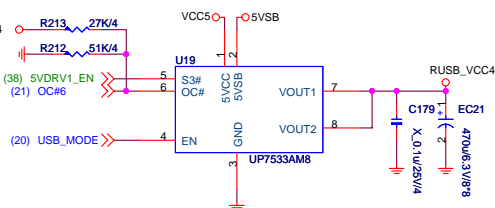
USB POWER FOR PORT 4, 5



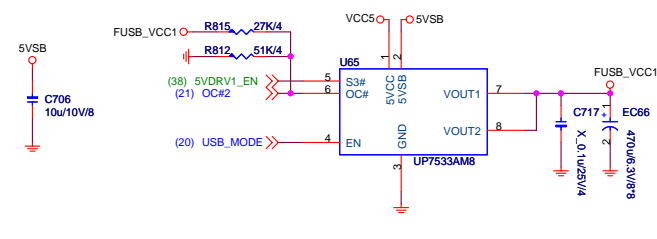
USB POWER FOR PORT 2,3



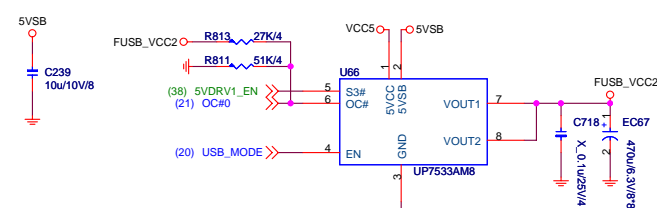
USB POWER FOR PORT 6,7



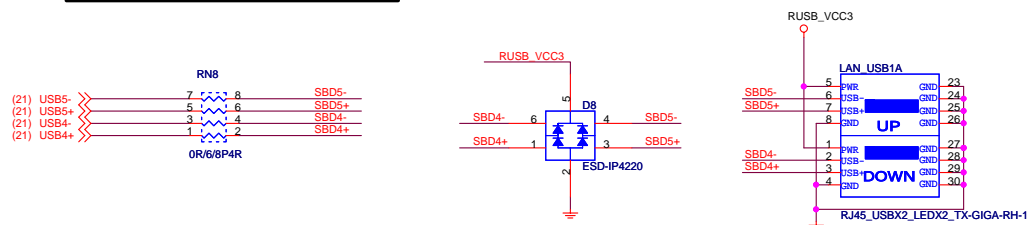
USB POWER FOR PORT 8,9



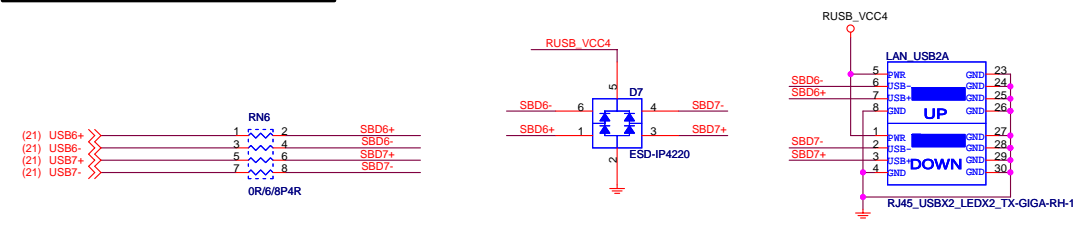
USB POWER FOR PORT 10,11



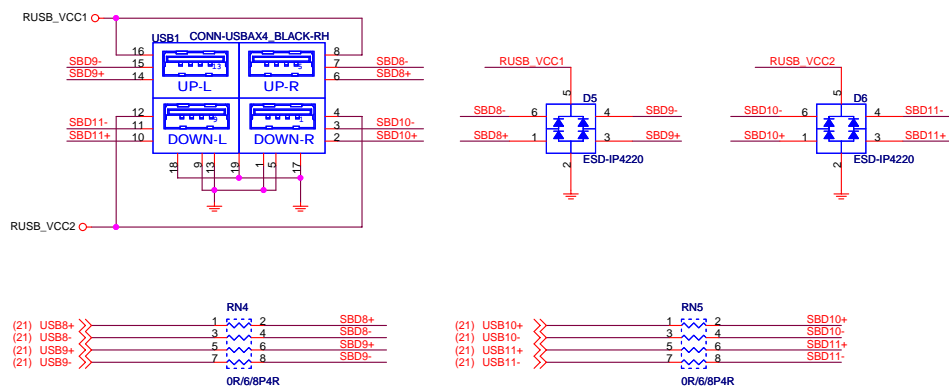
REAR USB PORT 4,5 (With LAN)



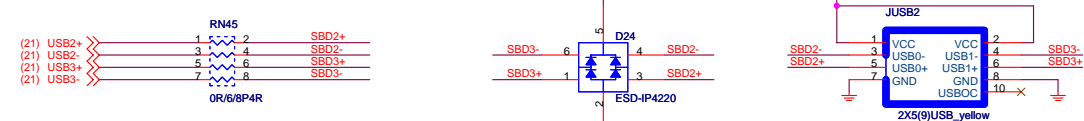
REAR USB PORT 6,7 (With LAN)



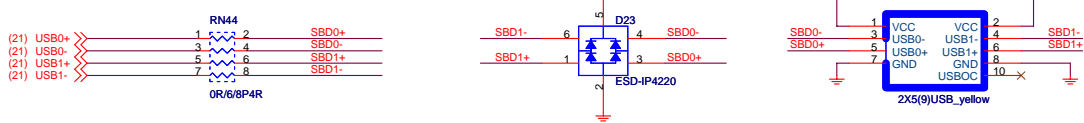
REAR USB PORT 0,1,2,3 (2x2)



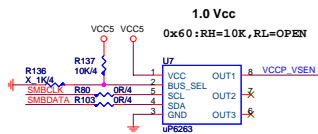
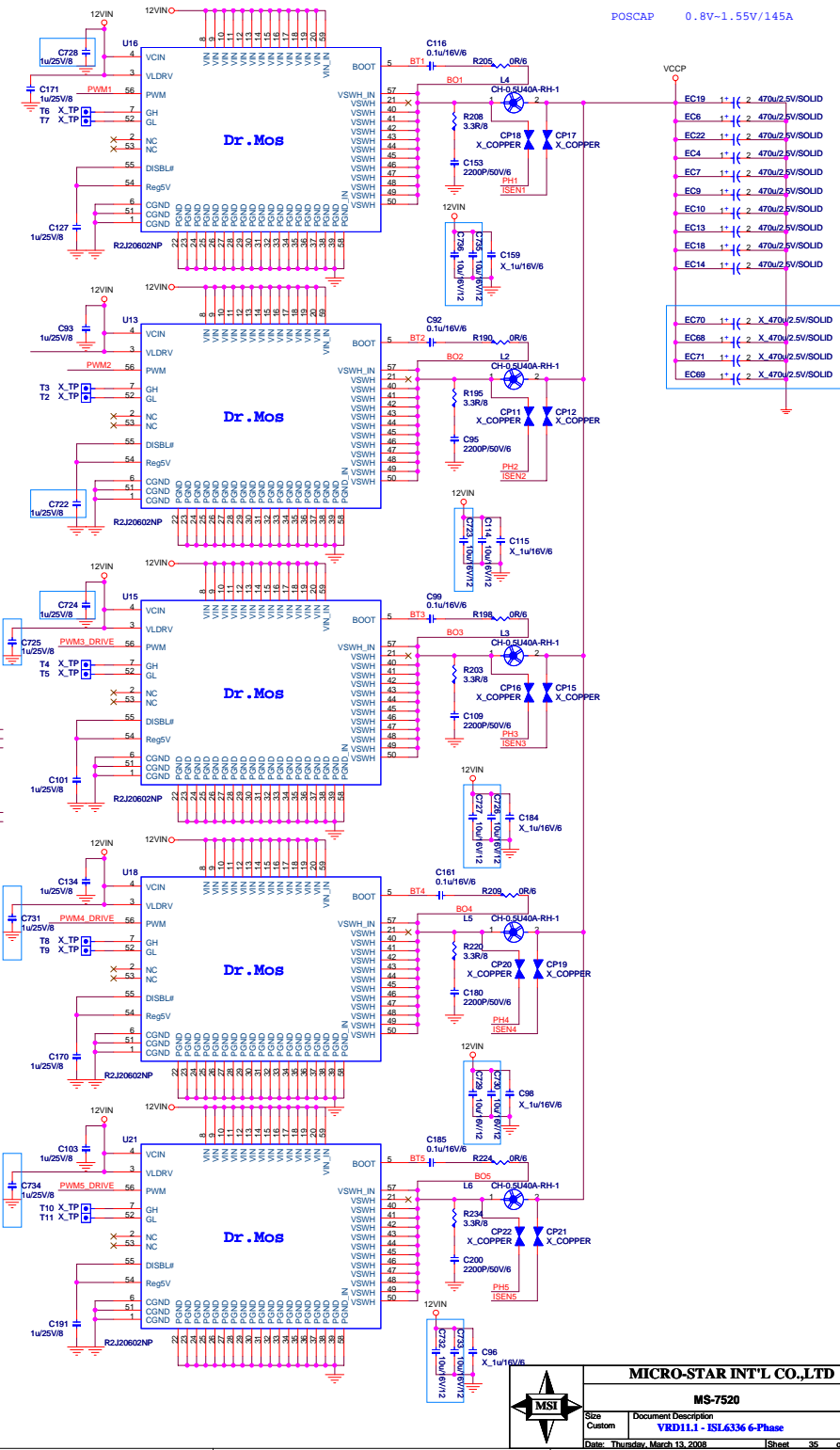
FRONT USB PORT 8,9



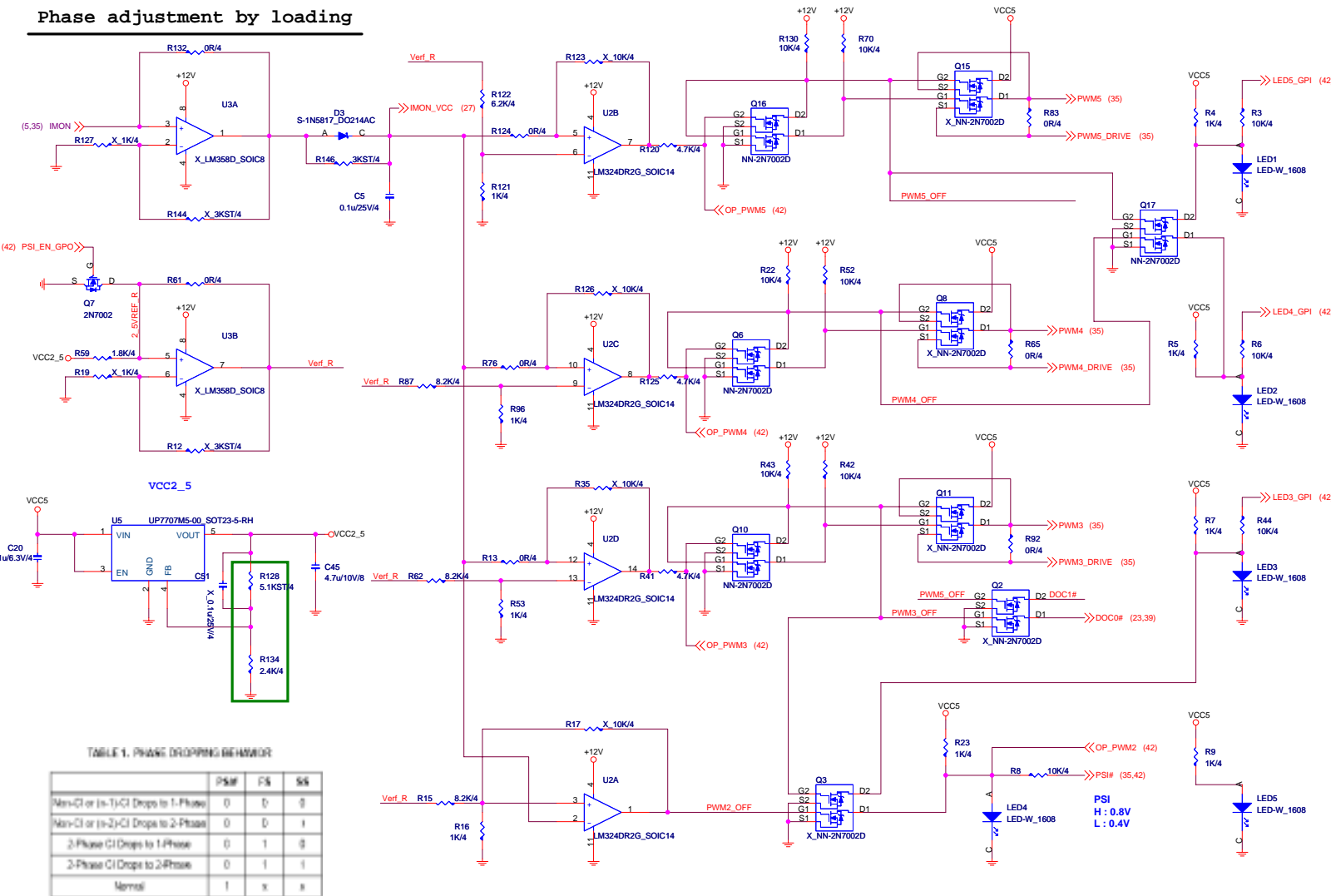
FRONT USB PORT 10,11



POSCAP 0.8V~1.55V/145A

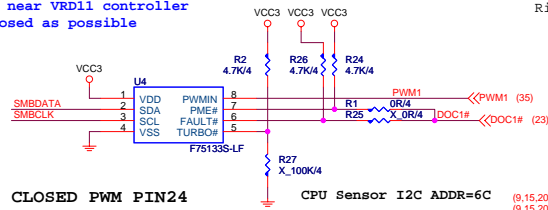


Phase adjustment by loading



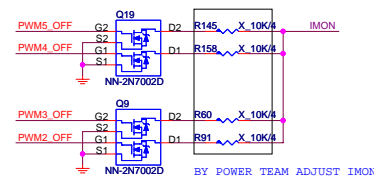
EASY DOT FUNCTION

Place near VRD11 controller as closed as possible

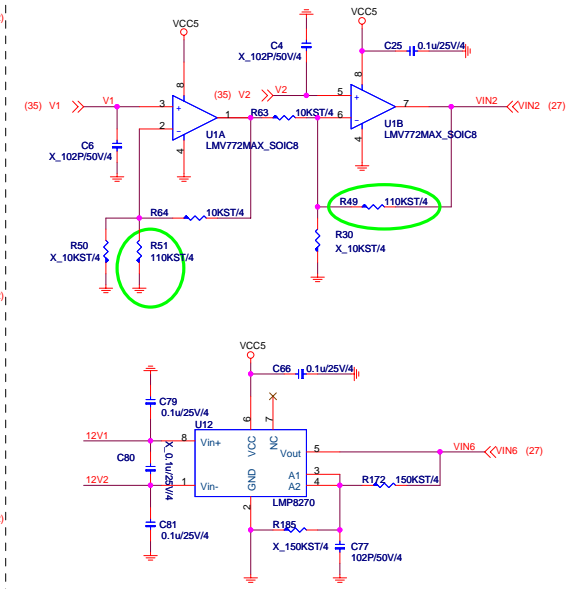


Vimom = (Riout / N) x (Rx/Risen) x Iload
 Riout = Rimom
 Rx = DCR
 Risen = ISEN+

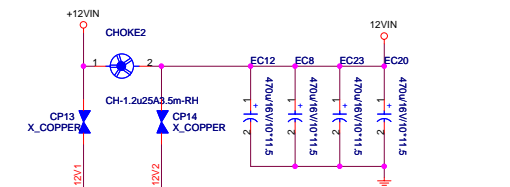
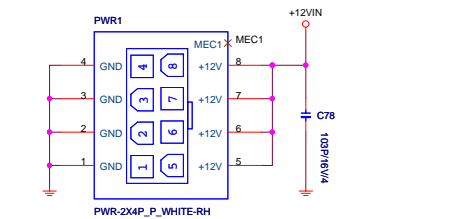
DOC#0	DOC#1	Over-clk
1	1	15%
0	1	10%
1	0	5%
0	0	Normal



Power Wattage Monitor



CPU +12VIN POWER CONN.



ISL6314CR POWER CKT FOR VTT 1.1V

VITPWRGD LEVEL SHIFT

VCC3 3VSB CPU_VTTD

R293 1K/4 R302 10K/4 R305 4.7K/4

Q30 NN-CMKT3904

C224 X_1u/6.3V/4 R304 X_0R/4 C229 1u/6.3V/4

(35) VTT_PGD_3V VTT_PGD

VCC3 R241 X_1K/4 (38) VR_VTT_EN R242 X_0R/4

(5) VTT_PGD VTT_PGD

(5) H_VTT_VID4 R251 0R/4 VTT_VID7

(5) H_VTT_VID3 R262 0R/4 VTT_VID6

(5) H_VTT_VID2 R268 0R/4 VTT_VID5

(9,15,20,23,25,26,32,33,35,36,38,39,40,42,43) SMBCLK X SMBCLK

(9,15,20,23,25,26,32,33,35,36,38,39,40,42,43) SMBDATA X SMBDATA

CPU_VTTD

R260 10K/4 VTT_VSEN

(5) VTT_SENSE R261 X_51/4

(5) VTT_VSS_SENSE

R269 100/4 C211 0.1u/25V/4 C212 X_0.1u/25V/4

V_6314

R300 100K/4 R283 X_2.7K/4

R299 X_100K/4 V_6314

R282 100K/4 R281 100K/4

C218 103P/16V/4

6X6 QFN

ISL6314CRZ_QFN32-RH

PGOOD EN VID7 VID6 VID5 VID4 VID3 VID2 VID1 VID0

PVCC BOOT UGATE PHASE LGATE

ISEN+ ISEN- VTT_ISEN+ VTT_ISEN- VTT_PHASE

ISENO

OCSET

NC

VDIFF

DVC

FB

COMP

APA

R245 2.2/8 C207 0.1u/16V/6

R253 4.7K/4 C208 0.1u/16V/6 C209 0.1u/25V/4

R252 23.7KST/4

R256 174RST/4 C210 102P/50V/4

R274 24.9RST/4 R273 1K/4 C217 820P/50V/4

R288 15KST/4 C220 102P/50V/4

C226 22P/50V/4 R295 12.1KST/4 C227 102P/50V/4

C216 102P/50V/4 R289 3KST/4

+12V_VTT

R277 10K/6 Q29 N-NTMFS4841

C235 10u/16V/12

18A

CHOKE5 CH-0.5u/40A0.81m-RH

CPU_VTTD

R318 2.2/8 CP25 X_COPPER VTT_PHASE

C233 2200P/50V/6 VTT_ISEN+

CP24 X_COPPER

CPU_VTTD

CHOKE6 CH-1.2U15A

+12V_VTT

EC33 470u/16V/10*11.5

VID 0 1 2 3 4 5 6 7

0 1 0 0 0 0 1 0 1.2V

0 1 1 0 0 0 1 0 1.175V

0 1 0 1 0 0 1 0 1.150V

0 1 1 1 0 0 1 0 1.125V

0 1 0 0 1 0 1 0 1.100V

0 1 0 1 1 0 1 0 1.070V

0 1 1 1 1 0 1 0 1.025V

VCC3 R279 X_1K/4 VTT_VID7 R280 1K/4

R247 1K/4 VTT_VID6 R248 X_1K/4

R249 X_1K/4 VTT_VID5 R250 1K/4

R254 X_1K/4 VTT_VID4 R255 1K/4

R258 X_1K/4 VTT_VID3 R259 1K/4

R263 X_1K/4 VTT_VID2 R264 1K/4

R266 1K/4 VTT_VID1 R267 X_1K/4

R271 X_1K/4 VTT_VID0 R272 1K/4

UPI VOLTAGE CONSOLE

0 Vcc

0x6A: RH=OPEN, RL=10K

VCC5 VCC5

R291 X_10K/4 R290 10K/4

SMBCLK R265 0R/4

SMBDATA R292 0R/4

U24

OUT1 VTT_VSEN

OUT2

OUT3

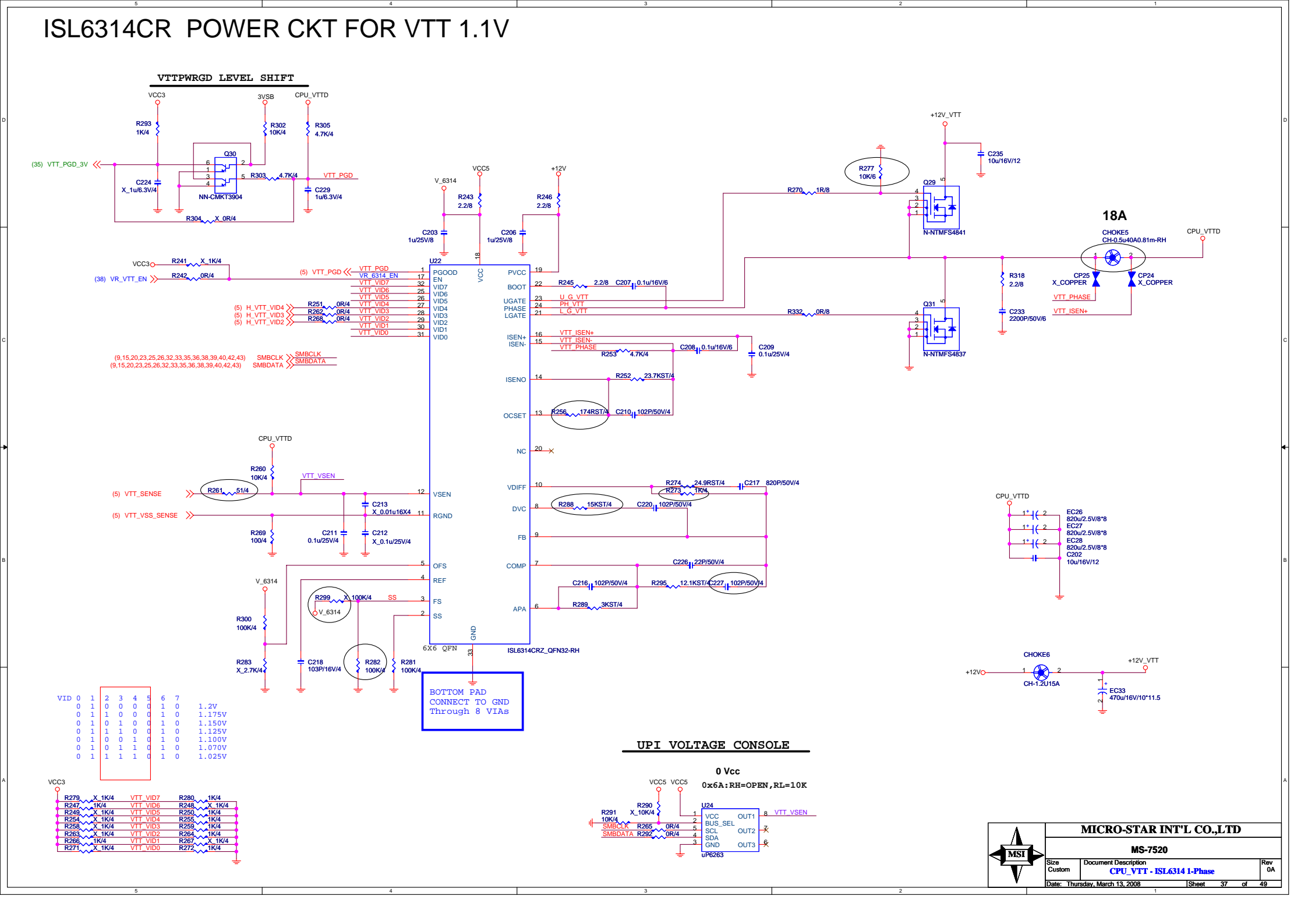
uP6263

MICRO-STAR INT'L CO.,LTD

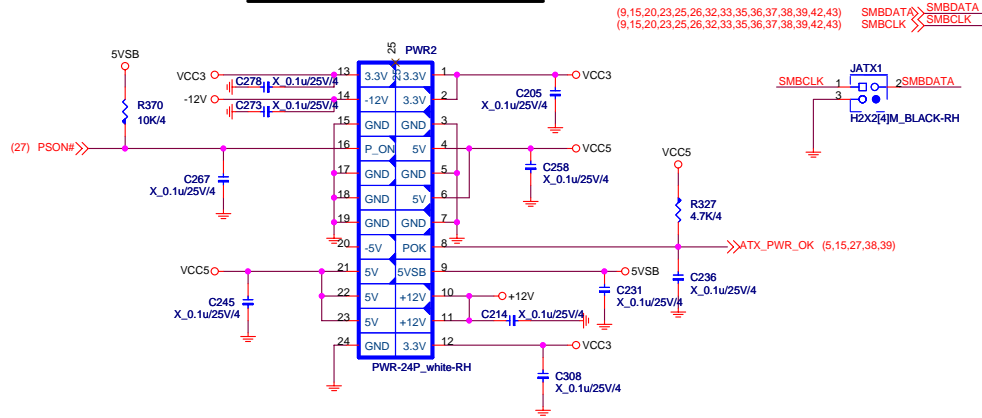
MS-7520

Size Custom Document Description CPU_VTT - ISL6314 1-Phase Rev 0A

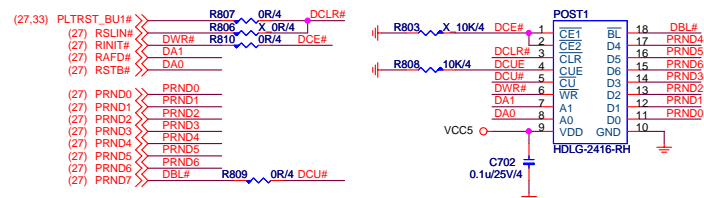
Date: Thursday, March 13, 2008 Sheet 37 of 49



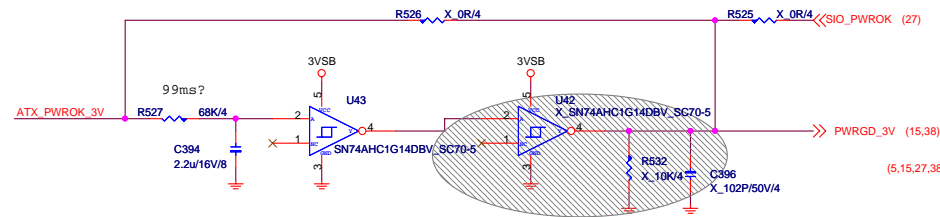
ATX POWER CONNECTOR



Debug Post Port



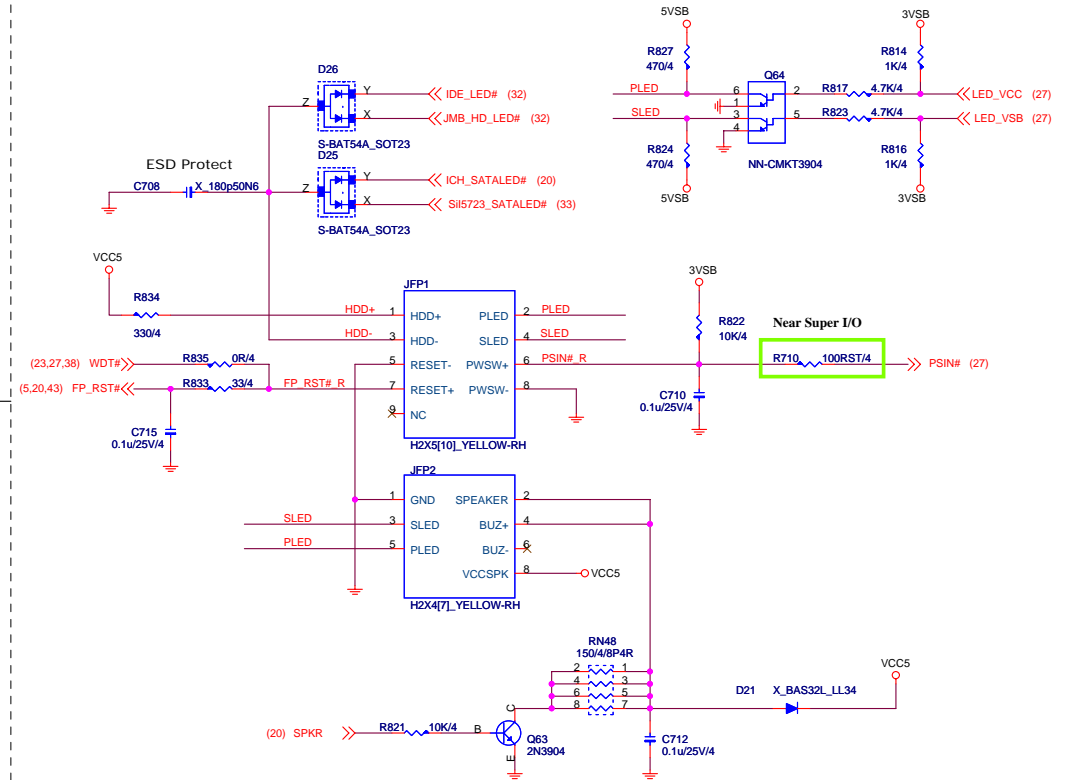
CHIPSET POWER GOOD CIRCUIT



FRONT PANNEL

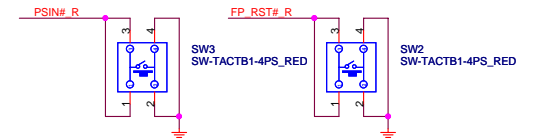
For MSI / Intel Front Panel

LED (By Fintek 71882)

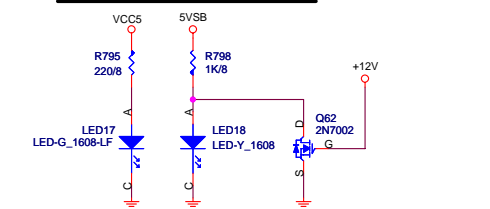


POWER ON BUTTON

RESET BUTTON

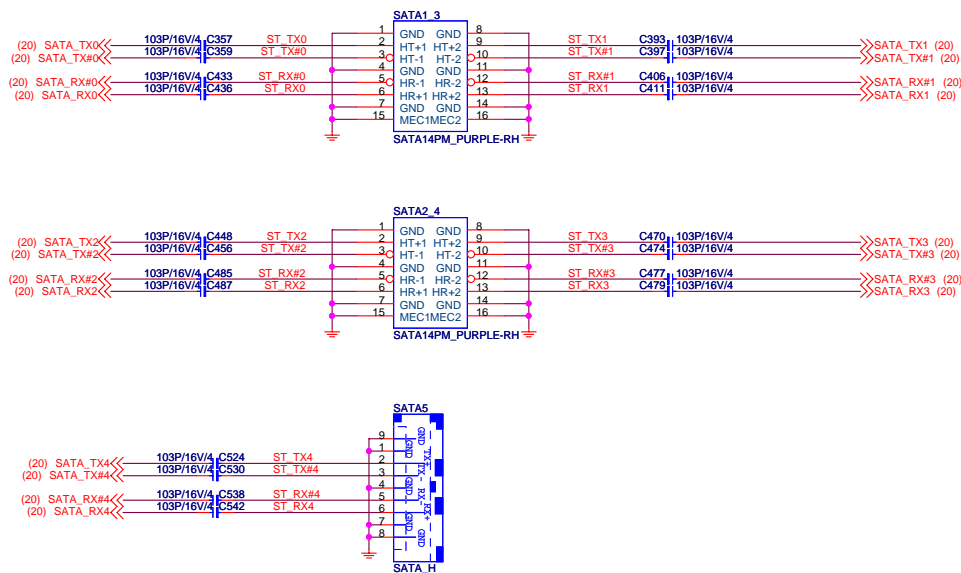


POWER LED (S0/S3)



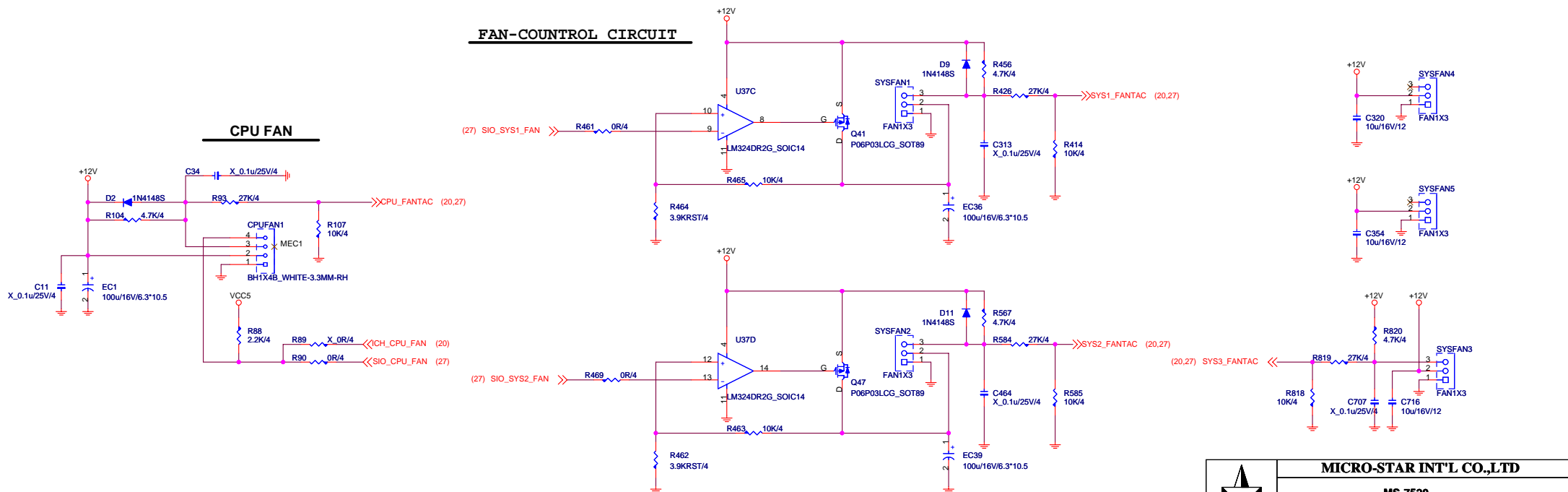
MICRO-STAR INT'L CO.,LTD			
MS-7520			
Size	Document Description	Rev	
Custom	ATX Connector/F_Panel	0A	
Date:	Thursday, March 13, 2008	Sheet	40 of 49

SATA-II Connector



FAN-COUNTROL CIRCUIT

CPU FAN



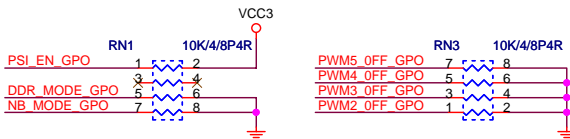
MICRO-STAR INT'L CO.,LTD

MS-7520

Size	Document Description	Rev
Custom	ICH SATA / FAN Control	0A
Date:	Thursday, March 13, 2008	Sheet 41 of 49

GPIO Controller

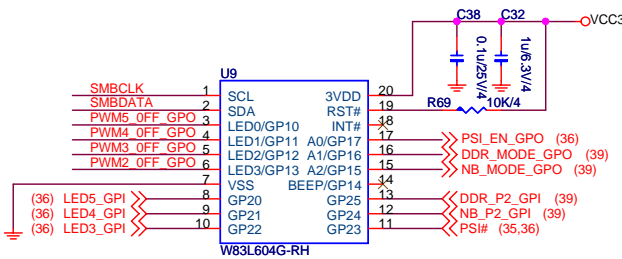
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(9,15,20,23,25,26,32,33,35,36,37,38,39,40,43)



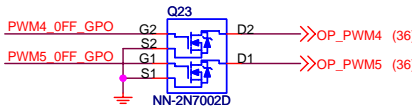
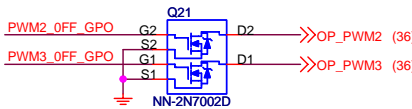
```

Programming
Default GPI ==>GPO(O/D)==>GPO(O)==>GPO(O)
          0          0          0          1

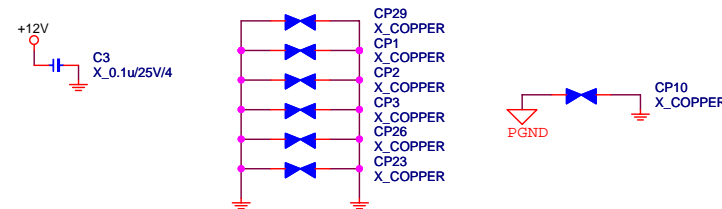
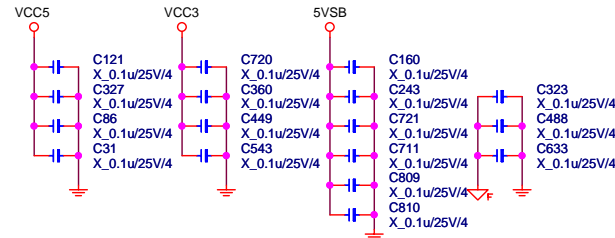
```



Only PSI_EN_GPO Default High
Others Default Low



EMI CAP



MICRO-STAR INT'L CO.,LTD

MS-7520

Size
Custom

Document Description

GPIO Controller/EM

Rev
0A

Date: Thursday, March 13, 2008

Sheet 42 of 49

CPU_VTDD **JDP_DEBU1**

43 VCC_OBS_AD
44 VCC_OBS_CB

PREQ# 3 OBSFN_A0
PRDY# 5 OBSFN_A1
3PM#0 9 OBSSDATA_A_0
3PM#1 11 OBSSDATA_A_1
3PM#2 15 OBSSDATA_A_2
3PM#3 17 OBSSDATA_A_3

X 21 OBSFN_B0
X 23 OBSFN_B1
3PM#4 27 OBSSDATA_B_0
3PM#5 29 OBSSDATA_B_1
3PM#6 33 OBSSDATA_B_2
3PM#7 35 OBSSDATA_B_3

51 SDA
53 SCL
4 OBSFN_C0
X 6 OBSFN_C1
X 10 OBSSDATA_C_0
X 12 OBSSDATA_C_1
X 18 OBSSDATA_C_2
X 18 OBSSDATA_C_3

X 22 OBSFN_D_0
X 24 OBSFN_D_1
X 28 OBSSDATA_D_0
X 30 OBSSDATA_D_1
X 34 OBSSDATA_D_2
X 36 OBSSDATA_D_3

61 X 61

62 X 62

TCK1 55
TK0 57
TDO 52
54
TRST# 56
TDI 58
TMS 58

HOOK0 39
HOOK1 41
HOOK2 45
HOOK3 47
ITPLCK/HOOK4 40
ITPLCKB/HOOK5 42
RESETB/HOOK6 46
DBR8/HOOK7 48

1
7
13
19
25
31
37
49
59
2
8
14
20
26
32
38
50
60
62

H TCK (5)
H TDO (5)
H TRST# (5)
H TDI (5)
H TMS (5)

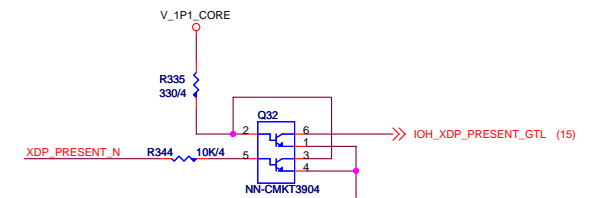
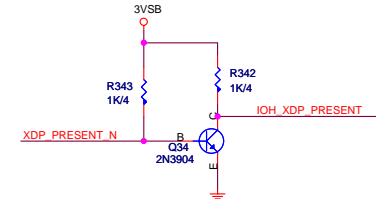
PRI_PWRGD_XDP (15)
CPU_TAPGOOD (5)
CK_CPU_ITP_DP (5)
CK_CPU_ITP_DN (5)
FPGA_H_CUPURST (15)
FP_RST# (5,20,40)

GND18_XDP_PRESENTB

BTB60PF-RH

Pin connection diagram for the BT606PF-RH device. The diagram shows connections for V_P8_PLL, JDP_DEBUG, and various I/O pins. It includes a table of pin numbers, device signals, and target signals with their respective pin numbers and functions.

Pin	Device Signal	Target Signal	Target Pin	Target Function
43	VCC_OBS_AB	VCC_OBS_AB	55	TCK1
44	VCC_OBS_CD	VCC_OBS_CD	57	TCK0
3	OBSFN_A0	OBSFN_A0	52	TDO
9	OBSFN_A1	OBSFN_A1	54	TRSTn
11	OBSDATA_A_0	OBSDATA_A_0	56	TDI
15	OBSDATA_A_1	OBSDATA_A_1	58	TMS
17	OBSDATA_A_2	OBSDATA_A_2	39	HOOK0
21	OBSFN_B0	OBSFN_B0	41	HOOK1
23	OBSFN_B1	OBSFN_B1	45	HOOK2
27	OBSDATA_B_0	OBSDATA_B_0	47	HOOK3
29	OBSDATA_B_1	OBSDATA_B_1	40	ITPCLK/HOOK4
33	OBSDATA_B_2	OBSDATA_B_2	42	ITPCLKB/HOOK5
35	OBSDATA_B_3	OBSDATA_B_3	46	RESETB/HOOK6
51	SDA	SDA	48	DBR/HOOK7
53	SCL	SCL	1	GND
4	OBSFN_C0	OBSFN_C0	7	GND
6	OBSFN_C1	OBSFN_C1	13	GND
10	OBSDATA_C_0	OBSDATA_C_0	19	GND
12	OBSDATA_C_1	OBSDATA_C_1	25	GND
16	OBSDATA_C_2	OBSDATA_C_2	31	GND
18	OBSDATA_C_3	OBSDATA_C_3	37	GND
22	OBSFN_D_0	OBSFN_D_0	49	GND
24	OBSFN_D_1	OBSFN_D_1	59	GND
28	OBSDATA_D_0	OBSDATA_D_0	2	GND
30	OBSDATA_D_1	OBSDATA_D_1	8	GND
34	OBSDATA_D_2	OBSDATA_D_2	14	GND
36	OBSDATA_D_3	OBSDATA_D_3	20	GND
22	OBSFN_D_0	OBSFN_D_0	26	GND
24	OBSFN_D_1	OBSFN_D_1	32	GND
28	OBSDATA_D_0	OBSDATA_D_0	38	GND
30	OBSDATA_D_1	OBSDATA_D_1	50	GND
34	OBSDATA_D_2	OBSDATA_D_2	60	XDP_PRESENT_N
36	OBSDATA_D_3	OBSDATA_D_3	62	GND

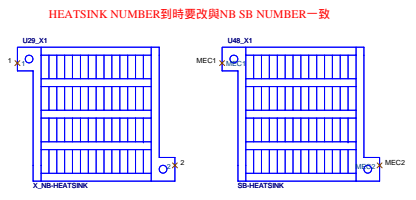
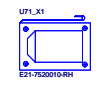
**MS-7520**

Size Custom	Document Description XDP PORT	Rev 0A
Date: Thursday, March 13, 2008	Sheet 43 of 49	

D

D

PCB1
7550
PD0-075200A-Y43, 育富,
PD0-075200A-G37, 精成



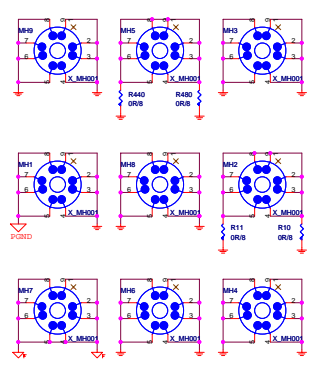
Optical Fiducial Marks-120



Optical Fiducial Marks-100



Mounting Holes



Simulation



B

B

A

A